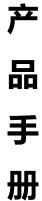


AGITERSERVICE



仪器型号: _____M8053A

西安安泰测试科技有限公司 仪器维修|租赁|销售|测试

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M8053A Interference Source 64 GHz

Version 1.0

Introduction

The Keysight M8053A interference source enables interference tolerance testing of highest-speed digital receivers supporting symbol rates above 64 GBd.



The M8053A Interference Source 64 GHz is a 2-slot AXIe module



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Overview

The M8053A interference source allows to generate repeatable and accurate level impairments for testing highest-speed digital receivers that support symbol rates above 64 GBd.



Figure 1. The screens show a 106.25 GBd PAM4 eye diagram without level interference (left) and with random level interference (right) added from M8053A. The example shows a PRBS13Q signal from M8050A high-performance BERT without ISI channel. The s-parameters of the coupler's main path have been de-embedded using the M8070ISIB.

Typical applications

The M8053A allows emulation of level interference for digital receiver tolerance testing. Typical applications that require sinusoidal or random interference signal are:

- PCIe 7/8 receiver testing
- Channel operating margin test for emerging Ethernet IEEE 802.3dj and ck
- Receiver interference tolerance test
- Optical receiver stress testing according to IEEE 802.3
- OIF CEI 112G and 224G receiver stress testing for medium and long reach



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Figure 2. The random interference signal provides a white gaussian noise with up to 64 GHz bandwidth. The upper part of the measurement shows a histogram taken with UXR1104A without attenuator. The lower part of the measurement shows that you can set the minimum and maximum bandwidth of the random interference signal. The spectral noise flatness is excellent within +- 2 dB.

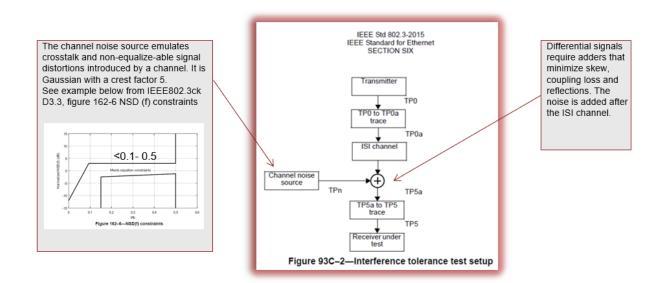




Figure 3. A typical interference tolerance test setup for Ethernet receivers. In this example a gaussian noise source, sometime also call a white noise source, is required for injecting level interference after the ISI channel. The example is from IEEE 802.3 – 2015, Annex 93C.

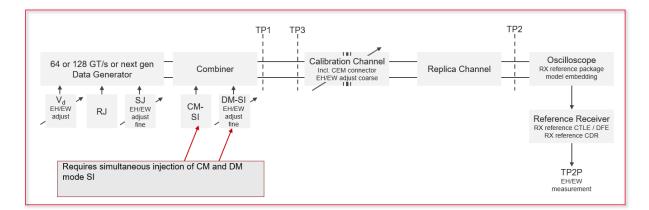


Figure 4. Typical PCI Express receiver stress calibration setup. It requires a simultaneous injection of common and differential mode sinusoidal interference before the channel.

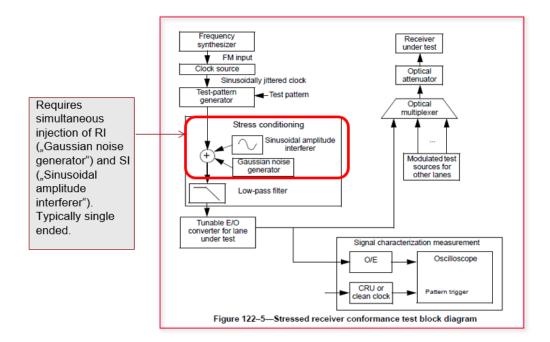


Figure 5. Typical optical stressed receiver sensitivity testing requires a simultaneous injection of random (gaussian noise) and sinusoidal interference. In most case a single ended signal is sufficient to drive the optical modulator.



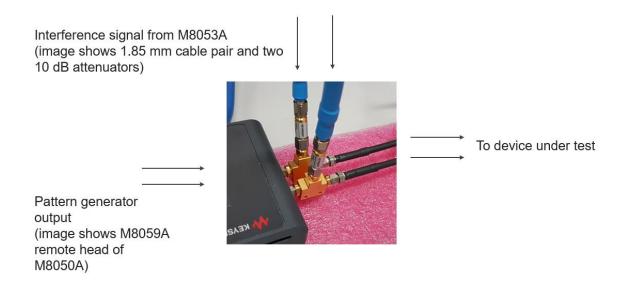


Figure 6. Keysight offers a matched coupler pair M8053A-803 to minimize differential skew and allow injection before and after the channel. The image shows prototypes.



Figure 7. The M8053A interference source can be configured with a M8050A high-performance BERT in one 5-slot AXIe chassis. The M8053A sits in the upper slot. It is also possible to configure the M8053A in a second AXIe chassis. The whole BERT system including the M8053A is controlled by the M8070B system software. This image shows prototype cables and coupler.



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M3: Module Auto Update is			SI1 State			SI2 Phase	
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RI Amplitude (RMS)	50.0 mV		SI2 State				🖆 🛃 🖆 🔊
RI Highest Frequency	53.000 GHz		SI2 Frequency	120.00 MHz		S-Parameter Profile	Factory/M8053A_Mod
RI Lowest Frequency	10.600 GHz		SI2 Amplitude (p-p)	900 mV		S-Parameter Output Port	
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Figure 8. The user interface of M8070B allows controlling all parameters of the M8053A interference source. This includes output amplitude, frequency, bandwidth. For de-embedding s2p and s4p files of the couplers, cables or other can be imported for each channel individually. This requires a M8070ISIB software license. It provides a graphical user interface and remote control.



Overview Interference Sources for High-Speed Digital Receiver Characterization

Keysight offers a choice of interference sources for testing high-speed digital receivers. The M8053A is for receiver characterization of highest speed digital receivers operating at symbol rates above 64 GBd. The following table gives an overview.

Model	Function	Description
M8053A Interference Source 64 GHz	The Keysight M8053 interference source enables interference tolerance testing of highest-speed digital receivers supporting symbol rates above 64 GBd. Recommended for 1.6T receiver stress testing and future generations of PCIe.	 RI and SI up to 64 GHz 2 differential channels 2-slot AXIe module Control from M8070B
M8054A Interference Source 32 GHz	The Keysight M8054A interference source, can be used as level interference source with sinusoidal and random modulation (also called gaussian or white noise). Recommended for USB, PCIe, SATA, SAS, 400GbE receiver stress testing.	 RI and SI up to 32 GHz 4 differential channels 1-slot AXIe module Control from M8070B
M8195A/ M8196A/ M8194A Arbitrary Waveform Generators	The Keysight M8195/6/4A AWGs are flexible sources with wide bandwidth suitable for multiple applications. They can also be used as level interference source with sinusoidal and random modulation.	 RI and SI up to 25/ 32/ 40 GHz 4 differential channels 1-slot AXIe module Control from M8070B
81160A Pulse Function Arbitrary Noise Generator 500 MHz	High precision pulse generators enhanced with versatile signal generation, modulation and distortion capabilities. Recommended for automotive Ethernet with symbol rates < 10 GBd.	 Noise up to 160 MHz Sinewave up to 500 MHz Stand-alone instrument



Specifications

Output Channel 1, 2

Table 1. Characteristics for M8053A output channels 1 and 2

Parameter

Number of channels per M8053A module	2
Output type	Single-ended ¹ or differential
Impedance	50 Ω (nom)
Amplitude	See table 2
Coupling	AC
De-embedding	One s2p file per channel
Connector	1.0 mm female

1 Unused output must be terminated with 50 Ω to GND

Sinusoidal and random Interference

The Keysight M8053A interference source, can be used as level interference source with sinusoidal and random modulation (also called gaussian or white noise).

The M8000 system software controls the interference parameters such as amplitude, frequency, bandwidth. Keysight provides matched directional coupler pairs for injecting the RI or SI signal before or after the channel (see recommended accessories).



Output channel 1,2

Table 2. Characteristics for outputs in interference mode

Mode	Parameter	
Amplitude ²		Peak-Peak amplitude s.e.: 0 mV to 1.25 V, 1 mV resolution Sum of RI, SI1, SI2 amplitudes has to be within peak-peak amplitude range above.
Random Interference (RI)		Yes
	Amplitude ¹	Peak-Peak amplitude single ended: 0 mV to 1.25 V, 1 mV resolution. Rms amplitude: 0 to 89 mV (assuming a CF of 7 and sinusoidal inference if off.)
	Lowest frequency range	1 MHz to 64 GHz
	Highest frequency range	1 MHz to 64 GHz
	Crest factor (peak ratio)	> 5.
		The crest factor is defined as shown in the formula below:
		$CF = \frac{\max(\operatorname{abs}(Hist_{min}), \operatorname{abs}(Hist_{max})))}{W}$
		$Hist_{std dev}$
Differential mode (DMRI)		Yes.
Common mode (CMRI)		Yes, needs coupling of channel 1 and channel 2
Sinusoidal interference (SI)		Yes, two independent sources per channel
	Modulation frequency range	1 MHz to 64 GHz
	Phase range	-360 to +360 deg
Common mode sinusoidal interference		Yes
(CMSI)	# of tones	One and two tones. Sum of amplitude for tone and tone 2 has to be within amplitude range
Differential mode sinusoidal interference		Yes
(DMSI)	# of tones	One and two. Sum of amplitude for tone 1 and tone 2 has to be within amplitude range
	Channel coupling	Yes, for channel 1 and channel 2
	Amplitude correction factor	0 to 10. Multiplies amplitude setting for each channel up to the maximum allowed amplitude. Can be used to compensate for different losses per channel in channel coupling mode.

 2 Single ended into 50 $\Omega.$ At DAC output. Amplitude range doubles in differential mode.



Trigger output

A differential output that generates sub-rate clocks.

Table 4. Trigger output characteristics

Value Amplitude 500 mV s.e. typical, fixed Offset 0 V typical, fixed DC Coupling Mode Sub rate clock. Divider 128 to 4000 of clock generator rate, must be multiple of 2 Frequency accuracy ± 50 ppm Termination 50 Ω Connector 3.5 mm female

Reference clock input

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator.

Table 5. Reference clock input characteristics

Input amplitude	600 mVpp to 2 Vpp
Input frequency	10 MHz or 100 MHz (±1%). Sinewave or square wave
Termination	Single ended, 50 Ohm, AC coupled
Connector	SMA, female

Reference clock output 16G

This signal provides a clock of 15 to 16 GHz, sample rate divided by 16. It can be used for as clock input for the precision time base of a DCA.

Table 6. Reference clock output specifications

Parameter	Specification		
Clock frequency	15 to 16 GHz nominal		
Amplitude	1100 mV pp sinusoidal typical. AC coupled		
Termination	50 Ω nominal		
Termination voltage range	0 V		
Connector	SMA female		



Matched coupler pair M8053A-803



Figure 9. The matched coupler pair M8053A-803 allows injecting the interference signal into a differential data signal before and after the channel to emulate far end and near end injected interference. The matching helps to minimize the skew.

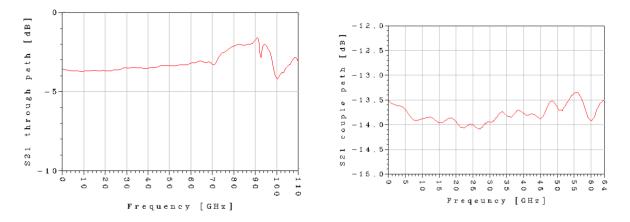


Figure 10. Typical insertion loss of the matched coupler pair for M8053A-803. The chart on the left shows the S21 of the through path and the chart on the right side shows the S21 of the coupling path.

Table 7. Coupler characteristics for M8053A-803

Parameter	
Bandwidth	Coupling path: 64 GHz typical Through path: 110 GHz typical
Insertion loss	Coupling path: - 14 dB typical at 60 GHz Through path: - 3 dB typical at 100 GHz
Skew	<1 ps
S-parameter	Typical s2p are available in M8070B factory folder for de-embedding.
Connector	Through: 1.0 mm (m), 1.0 mm (f) Coupling Path: 1.85 mm (f)



User interface and remote control

The M8070B system software for M8000 Series is required to control all parameters of M8053A.

Table 8. Software for the M8053A module

System software	Description
Controller requirements	M9537A 1-slot AXIe embedded controller, choose options for 10, 8 or 16GB RAM, SSD. External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub. number 5990-7632EN.
Operating System	Windows 10 (64 bit) Version 1607 (Anniversary update) or newer
Controller connectivity with AXIe chassis	USB 2.0 (mini-B) recommended. PCIe 2.0 (8x (only for highest data throughput and desktop PC)
Programming language	SCPI
Remote Control Interface	Desktop or Laptop PC: LAN M9537A: LAN
Save/Recall	Yes
Display resolution	Minimum 1024 x 768
Software pre-requisites	M8070B software revision 11.0.100.10 or later M8053A module driver 1.0 or later
	For de-embedding the s-parameters of the coupler, the M8070ISIB Adjustable ISI software package is required.
Software download	See for latest M8070B version: www.keysight.com/find/m8070b See for latest M8053A module driver version: https://www.keysight.com/us/en/support/M8053A/interference-source-64-ghz.html#drive

General characteristics and physical dimensions

Table 9. General characteristics for M8053A module

Parameter	Specification
Power consumption	220 W (nom)
Operating temperature	0 to 40°C
Operating humidity	15% to 95% relative humidity, non-condensing
Storage temperature	-40 to +70°C
Storage humidity	24 to 90 % relative humidity at 65°C (non-condensing)
Form factor	2-slot AXIe module



Dimensions (W x H x D)	351 mm x 60 mm x 309 mm	
Weight	5.95 kg	
Weight shipping	9.6 kg	
Safety designed to	IEC 61010-1, UL61010, CSA22.2 61010.1 tested	
EMC tested to	IEC 61326	
Warm-up time	30 min	
Calibration interval	2 years recommended	
Cooling requirements	When operating the M8053A choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side	



Ordering of M8053A

Table 10. Available options for M8053A

Description	Product number	
Interference source, 64 GHz, 2 channels, 2-slot AXIe module	M8053A	
RI and SI Interference, module-wide license	M8053A-0C1	
Extended 3- / 5-year warranty	R1280	
Calibration services (3 and 5 year)	R1282	

Default accessories included: four adapters 1.0 mm (m) to 1.85 mm (f), two 50 Ω terminations 2.4 mm and one 50 Ω termination 3.5mm, UK6 test report.

Table 11. Available accessories for M8053A

Description	Product number	Comment	
Matched cable pair, 1.85mm, length 850 mm, matching 1 ps	M8053A-801		
Matched coupler pair, Coupling path: bandwidth 64 GHz, coupling loss 14 dB, 1.85 mm Through path: bandwidth 110GHz, 3.5 dB, 1.0 mm	M8053A-803		
Adapter 1.0 mm (m) to 1.85 mm (f)	M8053A-804	Alternatively, Keysight 11921G	
Attenuator 10 dB, 1.85 mm	M8053A-805	Alternatively, Keysight 8490G-010	
Termination 50 Ohm, 1.0 mm	M8059A-802	For common mode we recommend 2 ea to terminate unused complement outputs of ch1 and ch2	
Termination 50 Ohm, 2.4 mm	M8199A-802		
Termination 50 Ohm, 3.5 mm	M8053A-806		

Chassis selection

The M8053A is shipped as stand-alone module.

M8053A can be used in M9505A, M9506A, and M9502A.



Specification

All specifications in this document are subject to change without notice.

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 - 40 °C and after a 30-minute warm up period.

Typical

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23 °C).

Nominal

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed.

Related Literature

M8050A	120 GBd High-performance BERT	Data Sheet	3122-1338.EN
M8040A	64 GBd High-performance BERT	Data Sheet	5992-1525EN
M8054A	Interference Source 32 GHz	Data Sheet	5992-3971EN
M8067A	ISI channel boards	Data Sheet	3122-2261.EN

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