PCI/PCIe/PXI/ PXIe/USB-6259 Specifications

2025-03-14

Contents

NI 6259 Specifications

Analog Input

Number of channels	16 differential or 32 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to the AI Absolute Accuracy section
Sample rate	
Single channel maximum	1.25 MS/s
Multichannel maximum (aggregate)	1.00 MS/s
Minimum	No minimum
Timing resolution	50 ns
Timing accuracy	50 ppm of sample rate
Input coupling	DC

Input range		±0.1 V, ±0.2 V, ±0.5 V, ±1 V, ±2 V, ±5 V, ±10 V
Maximum working voltage for analog inputs (signal + common mode)		±11 V of AI GND
CMRR (DC to 60 Hz)		100 dB
Input impedance		
Device on		
AI+ to AI GND	>10 GΩ in parallel with 100 pF	
AI- to AI GND	>10 GΩ in parallel with 100 pF	
Device off		
AI+ to AI GND		820 Ω
AI- to AI GND		820 Ω
Input bias current		±100 pA
Crosstalk (at 100 kHz)		
Adjacent channels		-75 dB
Non-adjacent channels		-95 dB

Small signal bandwidth (-3 dB)	1.7 MHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	
PCI/PCI Express/PXI/PXI Express	DMA (scatter-gather), interrupts, programmed I/O
USB	USB Signal Stream, programmed I/O
Overvoltage protection for all analog input and sense channels	
Device on	±25 V for up to four AI pins
Device off	±15 V for up to four AI pins
Input current during overvoltage condition	±20 mA maximum/AI pin

Settling Time for Multichannel Measurements

Table 1. Settling Time for Multichannel Measurements

Range	±60 ppm of Step (±4 LSB for Full-Scale Step)	±15 ppm of Step (±1 LSB for Full-Scale Step)
±1 V, ±2 V, ±5 V, ±10 V	1 µs	1.5 µs
±0.5 V	1.5 µs	2 µs
±0.1 V, ±0.2 V	2 µs	8 µs

Typical Performance Graphs

Figure 1. Settling Error versus Time for Different Source Impedances

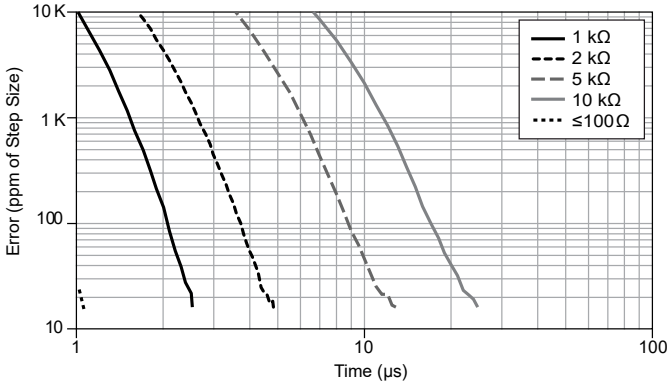


Figure 2. AI Small Signal Bandwidth

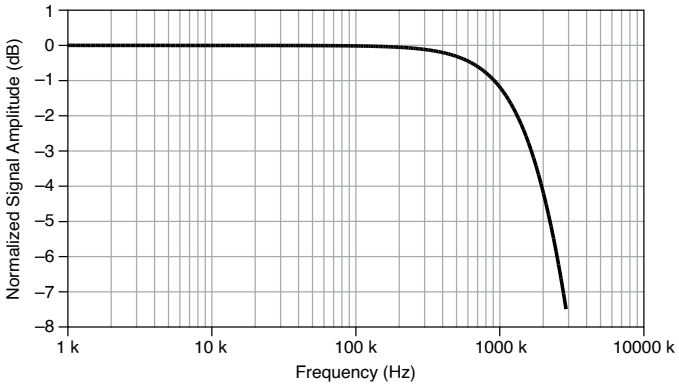
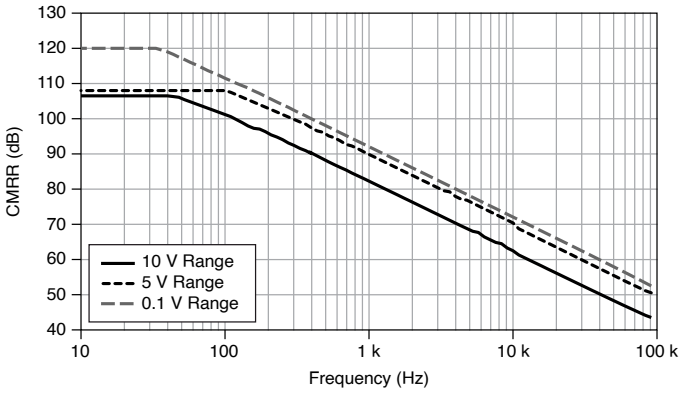


Figure 3. AI CMRR



AI Absolute Accuracy

Note Accuracies listed are valid for up to two years from the device external calibration.

Table 2. AI Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)	Sensitivity (µV)
10	-10	60	20	21	280	1,920	112.0
5	-5	70	20	21	140	1,010	56.0
2	-2	70	20	24	57	410	22.8
1	-1	80	20	27	32	220	12.8
0.5	-0.5	90	40	34	21	130	8.4
0.2	-0.2	130	80	55	16	74	6.4
0.1	-0.1	150	150	90	15	52	6.0

Note Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Gain tempco	13 ppm/°C
Reference tempco	1 ppm/°C
INL error	60 ppm of range

AI Absolute Accuracy Equation

$$AbsoluteAccuracy = Reading \cdot (GainError) + Range \cdot (OffsetError) + NoiseUncertainty$$

- $GainError = ResidualAIGainError + GainTempco \cdot (TempChangeFromLastInternalCal) + ReferenceTempco \cdot$

(TempChangeFromLastExternalCal)

- ***OffsetError*** = ***ResidualAIOffsetError*** + ***OffsetTempco*** · ***(TempChangeFromLastInternalCal)*** + ***INLError***
- ***NoiseUncertainty*** = $\frac{\text{Random Noise} \cdot 3}{\sqrt{100}}$ for a coverage factor of 3 σ and averaging 100 points.

AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- TempChangeFromLastExternalCal = 10 °C
- TempChangeFromLastInternalCal = 1 °C
- number_of_readings = 100
- CoverageFactor = 3 σ

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- GainError = 60 ppm + 13 ppm · 1 + 1 ppm · 10 = 83 ppm
- OffsetError = 20 ppm + 21 ppm · 1 + 60 ppm = 101 ppm
- NoiseUncertainty = $\frac{280\ \mu V \cdot 3}{\sqrt{100}}$ = 84 µV
- AbsoluteAccuracy = 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty = 1,920 µV

Analog Triggers

Number of triggers	1
Source	AI <0..31>, APFI <0, 1>

Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Source level	
AI <0..31>	±Full scale
APFI <0, 1>	±10 V
Resolution	10 bits, 1 in 1,024
Modes	Analog edge triggering, analog edge triggering with hysteresis, and analog window triggering
Bandwidth (-3 dB)	
AI <0..31>	3.4 MHz
APFI <0, 1>	3.9 MHz
Accuracy	±1%
APFI <0, 1> characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection, power on	±30 V

Protection, power off	±15 V

Analog Output

Number of channels	4
DAC resolution	16 bits
DNL	±1 LSB
Monotonicity	16 bit guaranteed
Accuracy	Refer to the AO Absolute Accuracy section

Maximum update rate	
1 channel	2.86 MS/s
2 channels	2.00 MS/s per channel
3 channels	1.54 MS/s per channel
4 channels	1.25 MS/s per channel

Timing accuracy	50 ppm of sample rate

Timing resolution	50 ns
Output range	±5 V, ±10 V, ±external reference on APFI <0, 1>
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA
Overdrive protection	±25 V
Overdrive current	20 mA
Power-on state	±5 mV [1]
Power-on glitch	1.5 V peak for 1.5 s
Output FIFO size	8,191 samples shared among channels used

Data transfers	
PCI/PCI Express/PXI/PXI Express	DMA (scatter-gather), interrupts, programmed I/O
USB	USB Signal Stream, programmed I/O

AO waveform modes	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full-scale step, 15 ppm (1 LSB)	2 µs
Slew rate	20 V/µs

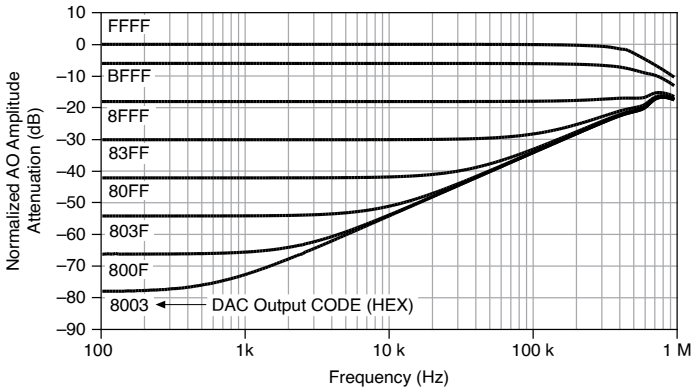
Glitch energy at midscale transition, ±10 V range	
Magnitude	10 mV
Duration	1 µs

External Reference

APFI <0,1> characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection, device on	± 30 V
Protection, device off	± 15 V
Range	± 11 V

Slew rate	20 V/µs

Figure 4. AO External Reference Bandwidth



AO Absolute Accuracy

Absolute accuracy at full-scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration.

Note Accuracies listed are valid for up to two years from the device external calibration.

Table 3. AO Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Absolute Accuracy at Full Scale (µV)
10	-10	75	17	40	2	2,080
5	-5	85	8	40	2	1,045

Reference tempco	1 ppm/°C

INL error	64 ppm of range

AO Absolute Accuracy Equation

$$AbsoluteAccuracy = OutputValue \cdot (GainError) + Range \cdot (OffsetError)$$

- $GainError = ResidualGainError + GainTempco \cdot (TempChangeFromLastInternalCal) + ReferenceTempco \cdot (TempChangeFromLastExternalCal)$
- $OffsetError = ResidualOffsetError + AOOffsetTempco \cdot (TempChangeFromLastInternalCal) + INLError$

Digital I/O/PFI

Static Characteristics

Number of channels	48 total, 32 (P0.<0..31>), 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection	±20 V on up to two pins[2]

Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..31>)
Port/sample size	Up to 32 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	2,047 samples
DI Sample Clock frequency	
PCI/PCI Express/PXI/PXI Express	0 MHz to 10 MHz, system and bus activity dependent
USB	0 MHz to 1 MHz, system and bus activity dependent
DO Sample Clock frequency	
PCI/PCI Express/PXI/PXI Express	
Regenerate from FIFO	0 MHz to 10 MHz
Streaming from memory	0 to 10 MHz, system and bus activity dependent
USB	
Regenerate from FIFO	0 MHz to 10 MHz
Streaming from memory	0 MHz to 1 MHz, system and bus activity dependent

Data transfers	
PCI/PCI Express/PXI/PXI Express	DMA (scatter-gather), interrupts, programmed I/O
USB	USB Signal Stream, programmed I/O
DI or DO Sample Clock source[3]	Any PFI, RTSI, AI Sample or Convert Clock, AO Sample Clock, Ctr n Internal Output, and many other signals

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Recommended Operating Conditions

Level	Minimum	Maximum
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V
Output high current (I_{OH}) P0.<0..31>	—	-24 mA
Output high current (I_{OH}) PFI <0..15>/P1/P2	—	-16 mA
Output low current (I_{OL}) P0.<0..31>	—	24 mA

Level	Minimum	Maximum
Output low current (I_{OL}) PFI <0..15>/P1/P2	—	16 mA

Note On earlier versions of the USB-6259 Screw Terminal (part numbers 194021B/C/-0***x***), the digital I/O characteristics of P0.<16..31> match the characteristics of PFI <0..15>. Refer to the November 2006 version of the ***NI 625x Specifications*** (part number 371291G-01) for more details.

Electrical Characteristics

Level	Minimum	Maximum
Positive-going threshold (VT+)	—	2.2 V
Negative-going threshold (VT-)	0.8 V	—
Delta VT hystersis (VT+ - VT-)	0.2 V	—
I_{IL} input low current (V_{in} = 0 V)	—	-10 µA
I_{IH} input high current (V_{in} = 5 V)	—	250 µA

Digital I/O Characteristics

Figure 5. P0.<0..31>: I_{oh} versus V_{oh}

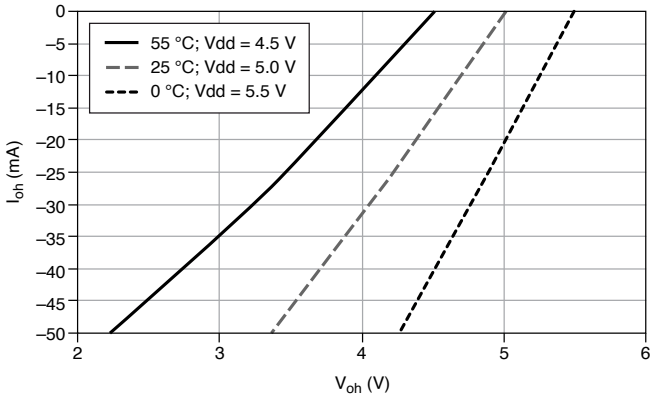


Figure 6. PFI <0..15>/P1/P2: I_{oh} versus V_{oh}

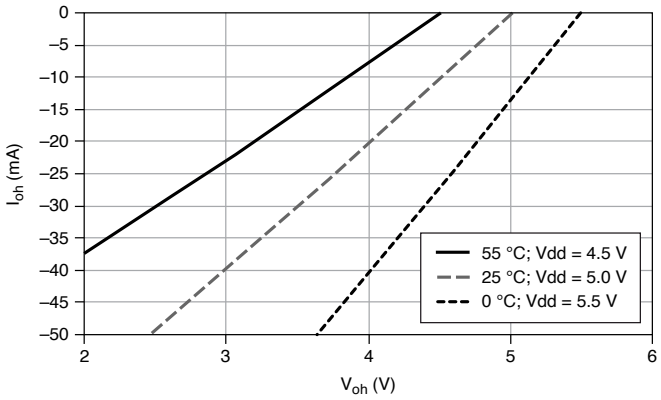


Figure 7. P0.<0..31>: I_{ol} versus V_{ol}

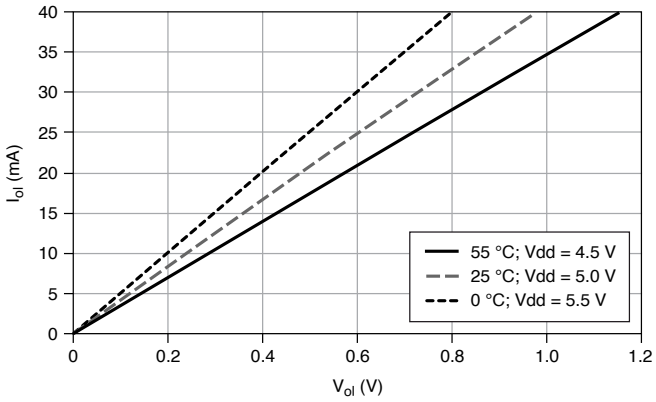
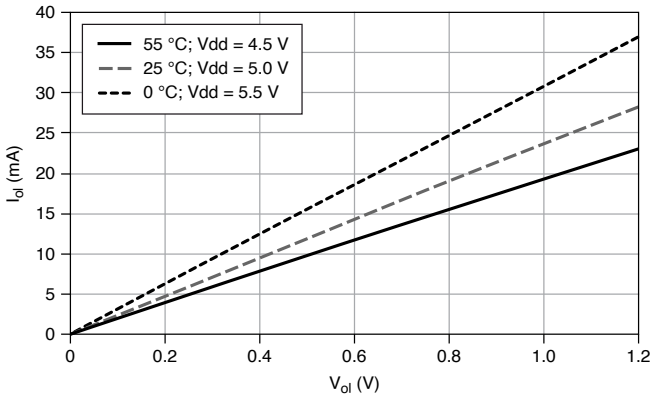


Figure 8. PFI <0..15>/P1/P2: I_{ol} versus V_{ol}



Note On earlier versions of the USB-6259 Screw Terminal (part numbers 194021B/C-0x), the digital I/O characteristics of P0.<16..31> match the characteristics of PFI <0..15>. Refer to the November 2006 version of the ***NI 625x Specifications*** (part number 371291G-01) for more details.

General-Purpose Counters/Timers

Number of counter/ timers	2
Resolution	32 bits
Counter measurements	Edge counting, pulse, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	80 MHz, 20 MHz, 0.1 MHz
External base clock frequency	0 MHz to 20 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Routing options for inputs	Any PFI, RTSI, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
FIFO	2 samples

Data transfers	
PCI/PCI Express/PXI/PXI Express	Dedicated scatter-gather DMA controller for each counter/timer; interrupts, programmed I/O
USB	USB Signal Stream, programmed I/O

Frequency Generator

Number of channels	1
Base clocks	10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm

Output can be available on any output PFI or RTSI terminal.

Phase-Locked Loop (PLL)

Note PCI/PCI Express/PXI/PXI Express devices only.

Number of PLLs	1
Reference signal	PXI_STAR, PXI_CLK10, RTSI <0..7>

Output of PLL	80 MHz Timebase; other signals derived from 80 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer function	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down
Digital waveform generation (DO) function	Sample Clock
Digital waveform acquisition (DI) function	Sample Clock

Device-to-Device Trigger Bus

PCI/PCI Express	RTSI <0..7>[4]

PXI/PXI Express	PXI_TRIG <0..7>, PXI_STAR
USB source	None
Output selections	10 MHz Clock, frequency generator output, many internal signals
Debounce filter settings	125 ns, 6.425 µs, 2.56 ms, disable; high and low transitions; selectable per input

Bus Interface

PCI/PXI	3.3 V or 5 V signal environment
PCI Express	
Form factor	x1 PCI Express, specification v1.0a compliant
Slot compatibility	x1, x4, x8, and x16 PCI Express slots[5]
PXI Express	
Form factor	x1 PXI Express peripheral module, specification rev 1.0 compliant
Slot compatibility	x1 and x4 PXI Express or PXI Express hybrid slots
USB	USB 2.0 Hi-Speed or full-speed[6], [7]

DMA channels (PCI/PCI Express/PXI/PXI Express)	6, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1
USB Signal Stream	4, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1

The PXI device supports one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

Table 4. PXI/SCXI Combo and PXI Express Chassis Compatibility

M Series Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
191325D-01/191325E-01L	No	Yes
191325D-11/191325E-11L	Yes	No
191325C-0x/191325B-0x	Yes	No

The PXI Express device can be installed in PXI Express slots or PXI Express hybrid slots.

Power Requirements

Current draw from bus during no-load condition[8]	
PCI/PXI	
+5 V	0.03 A
+3.3 V	0.725 A
+12 V	0.35 A

PCI Express	
+3.3 V	0.925 A
+12 V	0.35 A
PXI Express	
+3.3 V	0.45 A
+12 V	0.5 A
Current draw from bus during AI and AO overvoltage condition[8]	
PCI/PXI	
+5 V	0.03 A
+3.3 V	1.2 A
+12 V	0.38 A
PCI Express	
+3.3 V	1.4 A
+12 V	0.38 A
PXI Express	
+3.3 V	0.48 A

+12 V	0.71 A

Caution USB devices must be powered with an NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

USB power supply requirements	11 to 30 VDC, 20 W, locking or non-locking power jack with 0.080 in. diameter center pin, 5/16-32 thread for locking collars

Current Limits

Caution Exceeding the current limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI	
+5 V terminal (connector 0)	1 A maximum[9]
+5 V terminal (connector 1)	1 A maximum[9]
PCI Express	
Without disk drive power connector installed	
+5 V terminals combined	0.35 A maximum[9]
P0/PFI/P1/P3 and +5 V terminals combined	0.39 A maximum
With disk drive power connector installed	

+5 V terminal (connector 0)	1 A maximum[9]
+5 V terminal (connector 1)	1 A maximum[9]
P0/PFI/P1/P2 combined	0.39 A maximum
PXI/PXI Express	
+5 V terminal (connector 0)	1 A maximum[9]
+5 V terminal (connector 1)	1 A maximum[9]
P0/PFI/P1/P2 and +5 V terminals combined	2 A maximum
USB	
+5 V terminal	1 A max[9]
P0/PFI/P1/P2 and +5 V terminals combined	2 A maximum
Power supply fuse	2 A, 250 V

Physical Characteristics

Dimensions	
PCI printed circuit board	10.6 cm × 15.5 cm(4.2 in. × 6.1 in.)

PXI/PXI Express printed circuit board	Standard 3U PXI
Screw Terminal (includes connectors)	26.67 cm × 17.09 cm × 4.45 cm(10.5 in. × 6.73 in. × 1.75 in.)
BNC (includes connectors)	28.6 cm × 17 cm × 6.9 cm(11.25 in. × 6.7 in. × 2.7 in.)
Mass Termination enclosure (includes connectors)	18.8 cm × 17.09 cm × 4.45 cm (7.4 in. × 6.73 in. × 1.75 in.)
USB OEM	Refer to the ***NI USB-622x/625x/628x OEM User Guide***

Weight	
PCI	162 g (5.6 oz)
PCI Express	175 g (6.1 oz)
PXI	233 g (8.2 oz)
PXI Express	221 g (7.8 oz)
USB Screw Terminal	1.24 kg (2 lb 11 oz)
USB Mass Termination	816 g (1 lb 12.8 oz)

USB OEM	172 g (6.1 oz)
I/O connectors	
PCI/PCI Express/ PXI/PXI Express	2 68-pin VHDCI
Mass Termination	2 68-pin SCSI

Calibration

Recommended warm-up time	
PCI/PXI/PCI Express/PXI Express	15 minutes
USB	30 minutes
Calibration interval	2 years

Maximum Working Voltage

Connect only voltages that are below these limits.

Channel-to-earth	11 V, Measurement Category I

Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of

equipment, circuits powered by regulated low-voltage sources, and electronics.

Caution Do not use for measurements within Categories II, III, or IV.

Note Measurement Categories CAT I and CAT O (Other) are equivalent. These test and measurement circuits are not intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

Environmental

Operating temperature	
PCI/PXI/PXI Express	0 °C to 55 °C
PCI Express	0 °C to 50 °C
USB	0 °C to 45 °C
Storage temperature	-20 °C to 70 °C
Humidity	10% RH to 90% RH, noncondensing
Maximum altitude	2,000 m
Pollution Degree (indoor use only)	2

Indoor use only.

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

CE Compliance CE

- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Device Pinouts

Figure 9. NI PCI/PCIe/PXI/PXIe-6259 Pinout

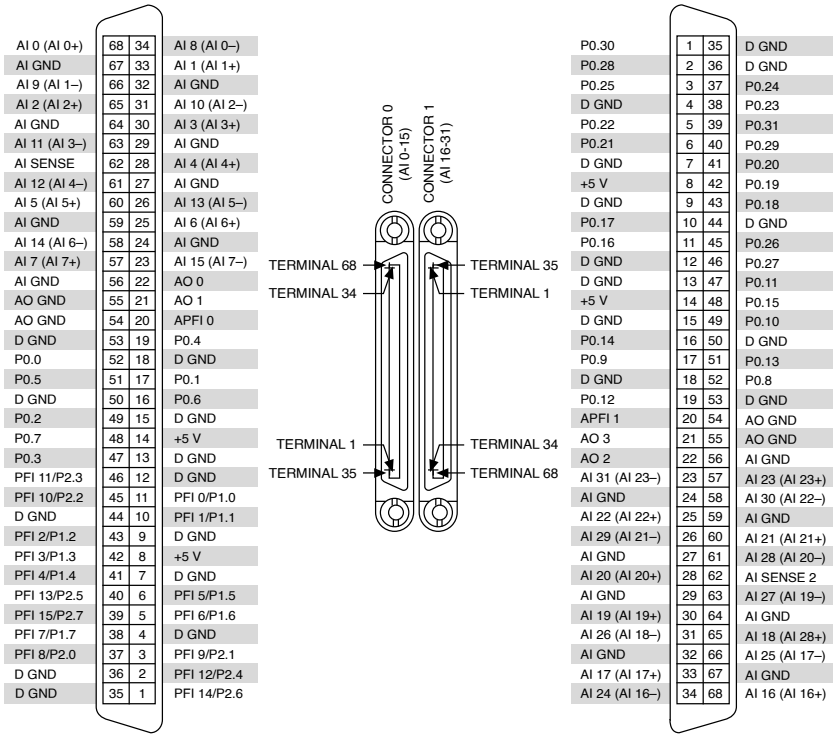


Figure 10. NI USB-6259 Screw Terminal Pinout

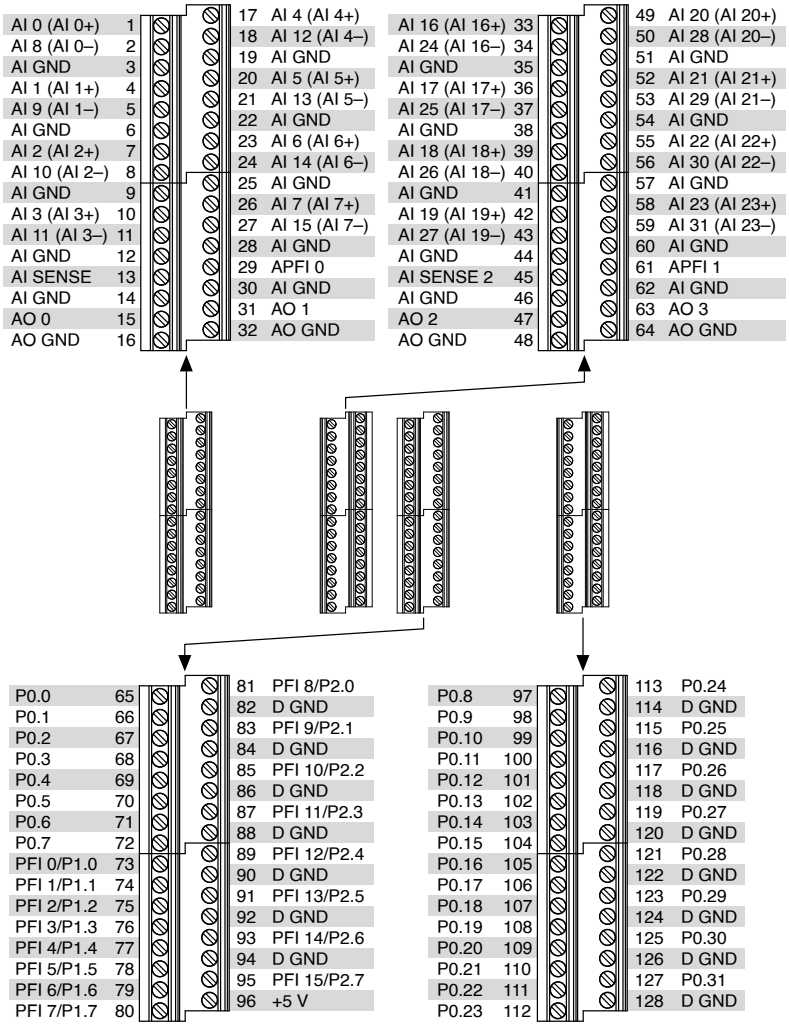


Figure 11. NI USB-6259 BNC Front Panel and Pinout

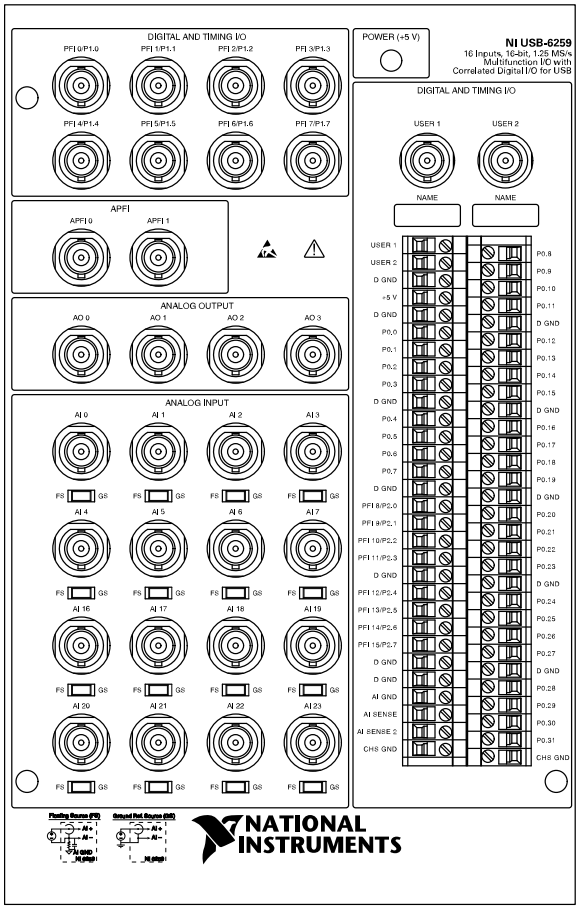
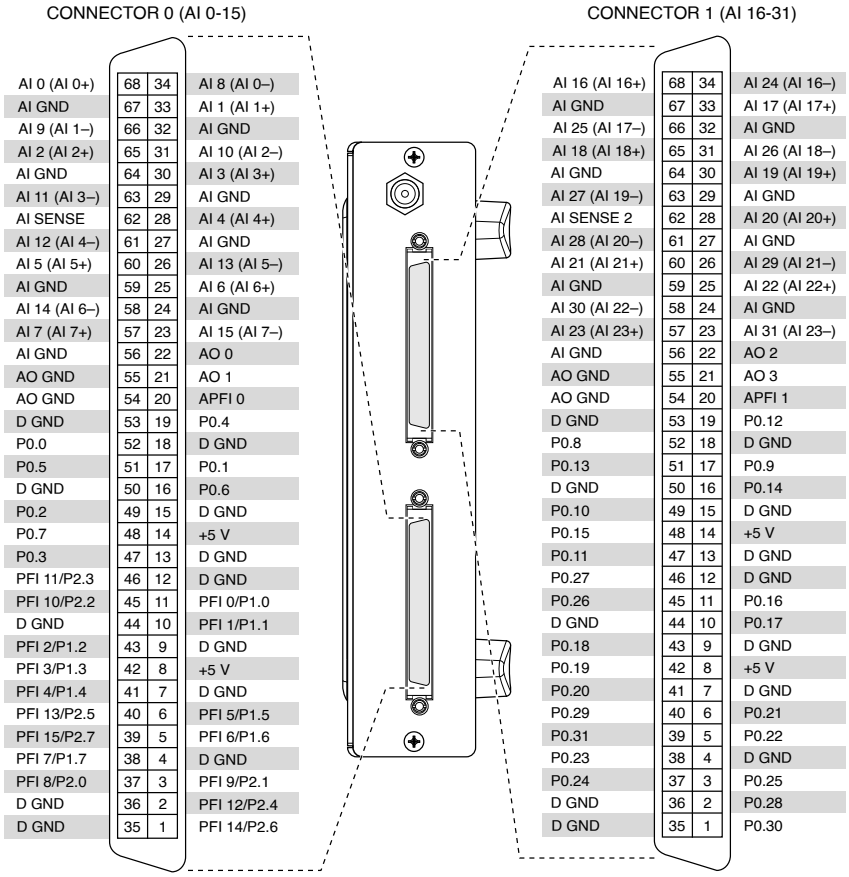


Figure 12. NI USB-6259 Mass Termination Pinout



CONNECTOR 0 (AI 0-15)				CONNECTOR 1 (AI 16-31)			
AI 0 (AI 0+)	68	34	AI 8 (AI 0–)	AI 16 (AI 16+)	68	34	AI 24 (AI 16–)
AI GND	67	33	AI 1 (AI 1+)	AI GND	67	33	AI 17 (AI 17+)
AI 9 (AI 1–)	66	32	AI GND	AI 25 (AI 17–)	66	32	AI GND
AI 2 (AI 2+)	65	31	AI 10 (AI 2–)	AI 18 (AI 18+)	65	31	AI 26 (AI 18–)
AI GND	64	30	AI 3 (AI 3+)	AI GND	64	30	AI 19 (AI 19+)
AI 11 (AI 3–)	63	29	AI GND	AI 27 (AI 19–)	63	29	AI GND
AI SENSE	62	28	AI 4 (AI 4+)	AI SENSE 2	62	28	AI 20 (AI 20+)
AI 12 (AI 4–)	61	27	AI GND	AI 28 (AI 20–)	61	27	AI GND
AI 5 (AI 5+)	60	26	AI 13 (AI 5–)	AI 21 (AI 21+)	60	26	AI 29 (AI 21–)
AI GND	59	25	AI 6 (AI 6+)	AI GND	59	25	AI 22 (AI 22+)
AI 14 (AI 6–)	58	24	AI GND	AI 30 (AI 22–)	58	24	AI GND
AI 7 (AI 7+)	57	23	AI 15 (AI 7–)	AI 23 (AI 23+)	57	23	AI 31 (AI 23–)
AI GND	56	22	AO 0	AI GND	56	22	AO 2
AO GND	55	21	AO 1	AO GND	55	21	AO 3
AO GND	54	20	APFI 0	AO GND	54	20	APFI 1
D GND	53	19	P0.4	D GND	53	19	P0.12
P0.0	52	18	D GND	P0.8	52	18	D GND
P0.5	51	17	P0.1	P0.13	51	17	P0.9
D GND	50	16	P0.6	D GND	50	16	P0.14
P0.2	49	15	D GND	P0.10	49	15	D GND
P0.7	48	14	+5 V	P0.15	48	14	+5 V
P0.3	47	13	D GND	P0.11	47	13	D GND
PFI 11/P2.3	46	12	D GND	P0.27	46	12	D GND
PFI 10/P2.2	45	11	PFI 0/P1.0	P0.26	45	11	P0.16
D GND	44	10	PFI 1/P1.1	D GND	44	10	P0.17
PFI 2/P1.2	43	9	D GND	P0.18	43	9	D GND
PFI 3/P1.3	42	8	+5 V	P0.19	42	8	+5 V
PFI 4/P1.4	41	7	D GND	P0.20	41	7	D GND
PFI 13/P2.5	40	6	PFI 5/P1.5	P0.29	40	6	P0.21
PFI 15/P2.7	39	5	PFI 6/P1.6	P0.31	39	5	P0.22
PFI 7/P1.7	38	4	D GND	P0.23	38	4	D GND
PFI 8/P2.0	37	3	PFI 9/P2.1	P0.24	37	3	P0.25
D GND	36	2	PFI 12/P2.4	D GND	36	2	P0.28
D GND	35	1	PFI 14/P2.6	D GND	35	1	P0.30