PCI-5124 Specifications

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PCI-5124 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. ***Warranted*** specifications account for measurement uncertainties, temperature drift, and aging. ***Warranted*** specifications are ensured by design, or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured (meas)*** specifications describe the measured performance of a representative model.

Specifications are ***Typical*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 200 MS/s using onboard clock
- The PCI-5124 module is warmed up for 15 minutes at ambient temperature.
- Calibration cycle is maintained.
- External calibration is performed at 23 °C ± 5 °C

Caution To ensure the specified EMC performance, operate this product only with double-shielded cables (for example, RG-233/U or equivalent) and shielded accessories.

Caution You can impair the protection provided by the PCI-5124 if you use it in a manner not described in this document.

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Connectors	BNC

Impedance and Coupling

Input impedance (software-selectable)	50 Ω ± 2.0% 1 MΩ ± 0.75% in parallel with a nominal capacitance of 29 pF
Input coupling (software-selectable)	AC[1] DC GND

Voltage Levels

Table 1. Full Scale (FS) Input Range and Programmable Vertical Offset

Range (V_{pk-pk})	Vertical Offset Range	
	50 Ω Input	1 MΩ Input
0.2 V	±0.1 V	
0.4 V	±0.2 V	
1 V	±0.5 V	
2 V	±1 V	
4 V	±2 V	
10 V	—	±5 V
20 V (1 MΩ only)	—	—

Maximum input overload	
50 Ω	7 V_{rms} with |Peaks| ≤10 V
1 MΩ	|Peaks| ≤42 V

Accuracy

Resolution	12 bits

Table 2. DC Accuracy[2], warranted

Range (V_{pk-pk})	Accuracy
0.2 V and 0.4 V	±(0.65% of input + 1.8 mV)
1 V and 2 V	±(0.65% of input + 2.1 mV)
4 V, 10 V, and 20 V[3]	±(0.65% of input + 10.0 mV)

Programmable vertical offset accuracy[4]	±0.4% of offset setting, warranted

Table 3. DC Drift, Nominal

Range (V_{pk-pk})	50 Ω and 1 MΩ
0.2 V, 0.4 V, 1 V, and 2 V	±(0.057% of input + 0.006% of FS + 100 µV) per °C
4 V, 10 V, and 20 V[3]	±(0.057% of input + 0.006% of FS + 900 µV) per °C

AC amplitude accuracy[4]	
50 Ω	±0.06 dB (±0.7%) at 50 kHz
1 MΩ	±0.09 dB (±1.0%) at 50 kHz
Crosstalk[5]	≤-85 dB at 10 MHz
Sparkle code rate[6]	
Onboard clock	<300 ppt [7]
External clock	
200 MHz	<300 ppt [7]
150 MHz	<3 ppt [7]
100 MHz	0

Bandwidth and Transient Response

Table 4. Bandwidth (±3 dB), Warranted[8], [9]

Input Range (V_{pk-pk}) [8]	50 Ω	1 MΩ
0.2 V	85 MHz	75 MHz
All other input ranges	150 MHz	145 MHz up to 40 °C[10]

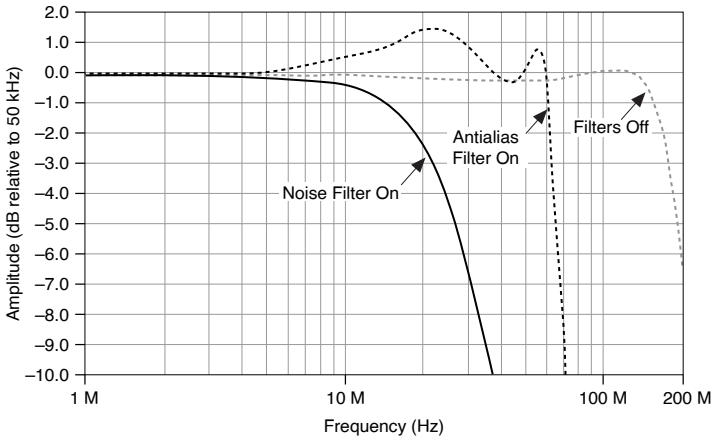
Rise/fall time[8]	
0.2 V_{pk-pk} input range	3.3 ns
All other input ranges	2.4 ns
Bandwidth limit filters[11]	
Noise filter	20 MHz 2-pole Bessel filter
Anti-alias filter	60 MHz 4-pole elliptical filter
AC coupling cutoff (-3 dB)[12]	12 Hz

Table 5. Passband Flatness[9]

Filter Settings[9]	Input Range (V_{pk-pk})	50 Ω and 1 MΩ
Filters off	0.2 V	±0.6 dB (DC to 20 MHz)

Filter Settings[9]	Input Range (V_{pk-pk})	50 Ω and 1 MΩ
		±1.5 dB (20 MHz to 40 MHz)
	All input ranges except 0.2 V	±0.5 dB (DC to 20 MHz) ±1.0 dB (20 MHz to 50 MHz) ±1.7 dB (50 MHz to 100 MHz)
Anti-alias filter on	All ranges	-1.0 dB to +2.0 dB (DC to 55 MHz)

Figure 1. PCI-5124 Frequency Response (Measured)



Spectral Characteristics

Table 6. Spurious-Free Dynamic Range with Harmonics (SFDR)[13]

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	75 dBc	70 dBc
0.4 V	75 dBc	70 dBc
1 V	72 dBc	70 dBc
2 V	72 dBc	70 dBc
4 V	65 dBc	67 dBc
10 V	65 dBc	60 dBc

Input Range (V_{pk-pk})	50 Ω	1 MΩ
20 V (1 MΩ only)	—	60 dBc

Table 7. Total Harmonic Distortion (THD)[14]

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	-74 dBc	-68 dBc
0.4 V	-74 dBc	-68 dBc
1 V	-72 dBc	-68 dBc
2 V	-72 dBc	-67 dBc
4 V	-63 dBc	-66 dBc
10 V	-63 dBc	-58 dBc
20 V (1 MΩ only)	—	-58 dBc

Intermodulation distortion (V_{pk-pk})[15]	-75 dBc

Table 8. Signal-to-Noise Ratio (SNR)[16]

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	57 dB	56 dB	53 dB	55 dB
0.4 V	58 dB	57 dB	55 dB	57 dB
1 V	58 dB	58 dB	57 dB	57 dB
2 V	58 dB	58 dB	57 dB	57 dB
4 V	—	—	56 dB	58 dB

Table 9. Signal to Noise and Distortion (SINAD)[17]

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	57 dB	56 dB	53 dB	55 dB
0.4 V	58 dB	57 dB	55 dB	57 dB
1 V	58 dB	58 dB	57 dB	57 dB
2 V	58 dB	58 dB	57 dB	57 dB
4 V	—	—	56 dB	57 dB

Figure 2. PCI-5124 Dynamic Performance, 50 Ω, 1 V Input Range, 262,144-Point FFT, Measured

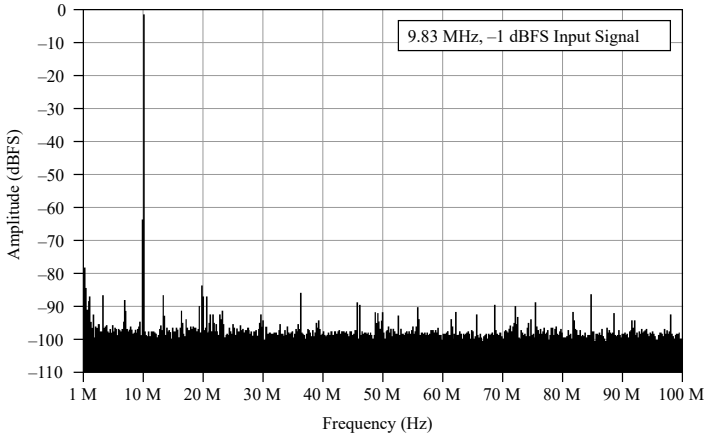


Table 10. RMS Noise (Noise filter on; 50 Ω terminator connected to input)

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	106 µVrms (0.053% FS)	116 µVrms (0.058% FS)
0.4 V	188 μV_{rms} (0.047% FS)	192 μV_{rms} (0.048% FS)
1 V	470 μV_{rms} (0.047% FS)	480 μV_{rms} (0.048% FS)
2 V	940 μV_{rms} (0.047% FS)	960 μV_{rms} (0.048% FS)
4 V	1.88 mV_{rms} (0.047% FS)	1.92 mV_{rms} (0.048% FS)
10 V	4.7 mV_{rms} (0.047% FS)	4.8 mV_{rms} (0.048% FS)
20 V (1 MΩ only)	—	9.4 mV_{rms} (0.047% FS)

Table 11. RMS Noise (Anti-alias filter on; 50 Ω terminator connected to input)

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	126 µVrms (0.063% FS)	146 µVrms (0.073% FS)
0.4 V	200 μV_{rms} (0.05% FS)	216 μV_{rms} (0.054% FS)
1 V	500 μV_{rms} (0.05% FS)	510 μV_{rms} (0.051% FS)
2 V	1.0 mV_{rms} (0.05% FS)	1.02 mV_{rms} (0.051% FS)
4 V	2.04 mV_{rms} (0.051% FS)	2.16 mV_{rms} (0.054% FS)
10 V	5.1 mV_{rms} (0.051% FS)	5.2 mV_{rms} (0.052% FS)
20 V (1 MΩ only)	—	10.2 mV_{rms} (0.051% FS)

Table 12. RMS Noise (Filters off; 50 Ω terminator connected to input)

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	128 µVrms (0.064% FS)	184 µVrms (0.092% FS)
0.4 V	204 μV_{rms} (0.051% FS)	264 μV_{rms} (0.066% FS)
1 V	510 μV_{rms} (0.051% FS)	550 μV_{rms} (0.055% FS)
2 V	1.02 mV_{rms} (0.051% FS)	1.08 mV_{rms} (0.054% FS)
4 V	2.08 mV_{rms} (0.052% FS)	2.6 mV_{rms} (0.065% FS)
10 V	5.2 mV_{rms} (0.052% FS)	5.5 mV_{rms} (0.055% FS)
20 V (1 MΩ only)	—	10.6 mV_{rms} (0.053% FS)

Figure 3. PCI-5124 Spectral Noise Density on 0.2 V Input Range, Noise Filter Enabled, 1 MΩ Input Impedance, Nominal

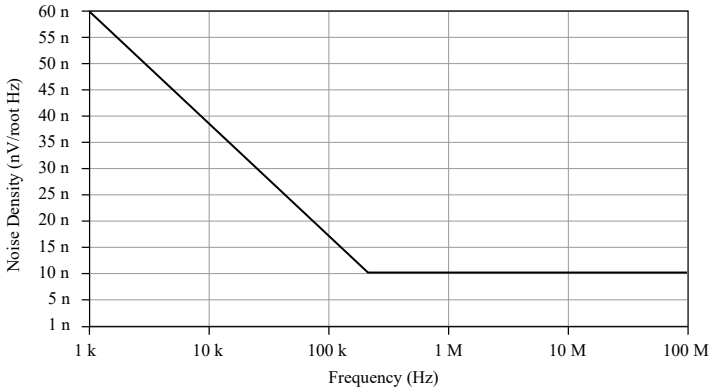
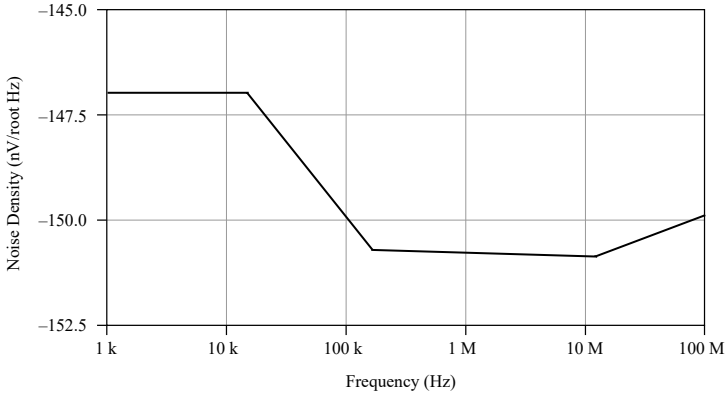


Figure 4. PCI-5124 Spectral Noise Density on 0.2 V Input Range, Full Bandwidth, 50 Ω Input Impedance, Nominal



Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCXO)[18]
External	CLK IN (front panel SMB connector)

Onboard Clock (Internal VCXO)

Sample rate range	
Real-time sampling (single shot)	3.052 kS/s to 200 MS/s[19]
Random interleaved sampling (RIS)	400 MS/s to 4 GS/s in multiples of 200 MS/s
Phase noise density[20]	<-100 dBc/Hz at 100 Hz <-120 dBc/Hz at 1 kHz

	<-130 dBc/Hz at 10 kHz
Sample clock jitter[21]	≤1 ps_{rms} (100 Hz to 100 kHz) ≤2 ps_{rms} (100 Hz to 1 MHz)
Timebase frequency	200 MHz
Timebase accuracy	
Not phase-locked to Reference clock	±25 ppm, Warranted
Phase-locked to Reference clock	Equal to the Reference clock accuracy
Sample clock delay range	±1 Sample clock period
Sample clock delay/adjustment resolution	≤5 ps

Related information:

- For more information about Sample clock and decimation, refer to the NI High-Speed Digitizers Help.

External Sample Clock

Sources	CLK IN (front panel SMB connector)
Frequency range[22]	50 MHz to 210 MHz (CLK IN)

Duty cycle tolerance	45% to 55%
Exported Reference clock destinations	CLK OUT (front panel SMB connector) PFI <0..1> (front panel 9-pinmini-circular DIN connector) RTSI <0..7>

Related information:

- For more information about Sample clock and decimation, refer to the NI High-Speed Digitizers Help.

Sample Clock Exporting

Table 13. Exported Sample Clock Destinations

Destination	Maximum Frequency
CLK OUT (front panel SMB connector)	210 MHz
PXI_Trig <0..6>[23]	20 MHz
PFI <0..1> (front panel 9-pinmini-circular DIN connector)[23]	25 MHz

Phase-Locked Loop (PLL) Reference Clock

Sources	RTSI 7 CLK IN (front panel SMB connector)
Frequency range	5 MHz to 20 MHz in 1 MHz increments[24]
Duty cycle tolerance	45% to 55%

Exported Reference clock destinations	CLK OUT (front panel SMB connector) PFI <0..1> (front panel 9-pinmini-circular DIN connector) RTSI <0..7>

CLK IN (Sample Clock and Reference Clock Input)

Connector	SMB jack
Input voltage range	
Sine wave (V_{pk-pk})	0.65 V to 2.8 V (0 dBm to 13 dBm)
Square wave (V_{pk-pk})	0.2 V to 2.8 V
Maximum input overload	7 V_{rms} with |Peaks| ≤10 V
Impedance	50 Ω
Coupling	AC

CLK OUT (Sample Clock and Reference Clock Output)

Connector	SMB jack
Output impedance	50 Ω

Logic type	3.3 V CMOS
Maximum drive current	±48 mA

Trigger

Reference (Stop) Trigger

Note Refer to the following sections and the ***NI High-Speed Digitizers Help*** for more information about what sources are available for each trigger type.

Trigger types	Edge Window Hysteresis Video Digital Immediate Software
Trigger sources	CH 0 CH 1 TRIG RTSI <0..6> Software

Time resolution		
Time-to-digital conversion circuit (TDC) on		
Onboard clock		50 ps
External clock		N/A
TDC off		
Onboard clock	5 ns	
External clock	External clock period	
Minimum rearm time[25]		
TDC on		10 µs
TDC off		2 µs
Holdoff		
Onboard clock		
TDC on	10 µs to 85.899 s	
TDC off	2 µs to 85.899 s	
External clock (TDC off)	200 × ***External clock period*** to (2^{32} - 1) × ***External clock period***	

Analog Trigger

Trigger types	Edge Window Hysteresis
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)
Trigger level range	
CH 0, CH 1	100% of FS
TRIG (External Trigger)	±5 V
Trigger level resolution	10 bits (1 in 1,024)
Edge trigger sensitivity, warranted	
CH 0, CH 1	3.5% FS up to 50 MHz Increases to 10% FS at 150 MHz
TRIG (external trigger), $V_{pk\text{-}pk}$	0.25 V up to 100 MHz Increases to 1 V at 200 MHz
Level accuracy	

CH 0, CH 1	±4.7% FS up to 10 MHz
TRIG (External Trigger)	±0.35 V up to 10 MHz
Trigger jitter	≤80 ps_{rms} [26]
Trigger filters	
Low-frequency (LF) reject	50 kHz
High-frequency (HF) reject	50 kHz

Digital Trigger

Trigger type	Digital
Sources	RTSI <0..6> PFI <0..1> (front panel SMB connector)

Video Trigger

Trigger type	Video
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)

Video trigger types	Specific line Any line Specific field
Standards	Negative sync of NTSC, PAL, or SECAM signal

External Trigger

Connector	TRIG (front panel BNC connector)
Impedance	1 MΩ in parallel with 22 pF
Coupling	AC DC
AC-coupling cutoff (-3 dB)	12 Hz
Input voltage range	±5 V
Maximum input overload	|Peaks| ≤42 V

PFI 0 and PFI 1 (Programmable Function Interface, AUX Front Panel Connectors)

Connector	9-pin mini-circular DIN
Direction	Bidirectional
As an input (trigger)	
Destinations	Start trigger (acquisition arm) Reference (stop) trigger Arm Reference trigger Advance trigger
Input impedance	150 kΩ, nominal
V_{IH}	2.0 V
V_{IL}	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz
As an output (event)	
Sources	Start trigger (acquisition arm)

	Reference (stop) trigger End of Record Done (end of acquisition) Probe Compensation[27]
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	±24 mA
Maximum frequency	25 MHz

Waveform Specifications

Onboard memory sizes	8 MB per channel (4 MS per channel) 32 MB per channel (16 MS per channel) 256 MB per channel (128 MS per channel)
Minimum record length	1 sample
Number of pretrigger samples	Zero up to full record length[28]
Number of posttrigger	Zero up to full record length[28]

samples	
Maximum number of records in onboard memory	
8 MB per channel	21,845
32 MB per channel	87,381
256 MB per channel	100,000[29]
Allocated onboard memory per record	(***Record Length*** × 2 bytes/S) + 200 bytes, rounded up to next multiple of 128 bytes or 384 bytes, whichever is greater

Calibration

External Calibration

External calibration calibrates the VCXO and the voltage reference. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[30]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE2.7.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-5124. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PCI-5124 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single

program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PCI-5124. MAX is included on the driver media.

Synchronization

Synchronization with the NI-TClk API [31]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PCI-5124 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PCI-5124 modules using NI-TClk [32]	
NI-TClk synchronization without manual adjustment [33]	
Skew, Peak-to-Peak [34]	500 ps
NI-TClk synchronization with manual adjustment [33]	
Skew after manual adjustment	<10 ps
Sample Clock delay/adjustment resolution	≤5 ps

Dimensions and Weight

Dimensions	35.5 cm × 2.0 cm × 11.3 cm (14.0 in × 0.8 in × 4.4 in)
Weight	455 g (16 oz)

Power

Current draw	
+3.3 VDC	1.3 A
+5 VDC	2.7 A
+12 VDC	130 mA
-12 VDC	0 A
Total power	19.4 W

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally

responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)