PXIe-6739 Specifications

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Contents

PXIe-6739 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are ***Typical*** unless otherwise noted.

Conditions

Specifications are valid at 25 °C unless otherwise noted.

Analog Output

Number of channels	64 voltage outputs
Resolution	16 bits, 1 in 65,536
DNL	±1.0 LSB maximum
Unscaled data format[1]	Unsigned integer (0 to 65,535)

Monotonicity	16 bits
Accuracy	Refer to the ***AO Absolute Accuracy*** table
Maximum update rate (using local FIFO)[2]	
1 channel	1 MS/s
16 channels (1 channel per bank) [3]	1 MS/s
64 channels [3]	350 kS/s
Timing accuracy (warranted)	50 ppm of sample rate
Timing resolution	10 ns
Output range	±10 V
Output coupling	DC
Output impedance	0.2 Ω
Output current drive[4]	±10 mA
Overdrive protection	±15 V

Overdrive current	15 mA
Power-on state	±200 mV
Power-on/off glitch	2.5 V peak for 100 ms
FIFO buffer size	65,535 samples shared among channels used
Data transfers	DMA (scatter-gather), programmed I/O

AO waveform modes

- Nonperiodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

Settling time, full scale step	15 µs to ±4 LSB
Slew rate	3.0 V/µs
Noise	1.0 mV RMS, DC to 1 MHz
AO update glitch	
Magnitude	3.0 mV
Duration	10 µs

Glitch energy	3 nVs
Channel crosstalk	-65 dB with SHC68-68-A2 cable (generating a 10 V, 100 point sinusoidal at 100 kHz on the reference channel)
Output stability	Any passive load

Note AO update glitch is the glitch energy that occurs on all channels on the same bank as the result of a channel update, regardless of value. For example, if you update the value of AO 0, all channels within that bank AO <0..3> will experience this glitch regardless of whether their output voltages change.

Absolute Accuracy (Warranted)

Absolute accuracy at full-scale number is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.

Table 1. AO Absolute Accuracy

Nominal Range Positive Full Scale	Nominal Range Negative Full Scale	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Offset Tempco (ppm)	Residual Offset Error (ppm of Range)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale (µV)
10	-10	109	12	1	4	95	64	2,940

Note Accuracies listed are valid for up to two years from the device external calibration.

AO Absolute Accuracy Equation

$$AbsoluteAccuracy = OutputValue \cdot (GainError) + Range \cdot (OffsetError)$$

$$AbsoluteAccuracy = OutputValue \cdot (GainError) + Range \cdot (OffsetError)$$

GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)

OffsetError = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

OffsetError = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INL_Error

Digital I/O/PFI

Static Characteristics

Number of channels	20 total, 4 (P0.<0..3>), 16 (PFI<0..7>/P1.<0..7>, PFI <8..15>/P2.<0..7>)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection[5]	±20 V on up to two pins

Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..3>)
Port/sample size	Up to 4 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	255 samples

DI Sample Clock Frequency	0 to 10 MHz, system and bus activity dependent
DO Sample Clock frequency	
Regenerate from FIFO	0 to 10 MHz
Streaming from memory	0 to 10 MHz, system and bus activity dependent
Data transfers	DMA (scatter-gather), programmed I/O
Digital line filter settings	160 ns, 10.24 µs, 5.12 ms, disable

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Recommended Operating Conditions

Input high voltage (V_{IH})	2.2 V minimum, 5.25 V maximum
Input low voltage (V_{IL})	0 V minimum, 0.8 V maximum

Output high current (I_{OH})	
P0.<0..3>	-24 mA maximum
PFI <0..15>/PI<0..7>/P2.<0..7>	-16 mA maximum
Output low current (I_{OL})	
P0.<0..3>	24 mA maximum
PFI <0..15>/P1<0..7>/P2.<0..7>	16 mA maximum

Electrical Characteristics

Level	Minimum	Maximum
Positive-going threshold (VT+)	—	2.2 V
Negative-going threshold (VT-)	0.8 V	—
Delta VT hysteresis (VT+ - VT-)	0.2 V	—
I_{IL} input low current (V_{in} = 0 V)	—	-10 µA
I_{IH} input high current (V_{in} = 5 V)	—	250 µA

Digital I/O Characteristics

Figure 1. P0.<0..3>: I_{OH} versus V_{OH}

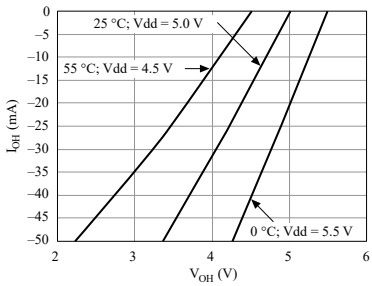


Figure 2. PFI <0..15>/PI/P2: I_{OH} versus V_{OH}

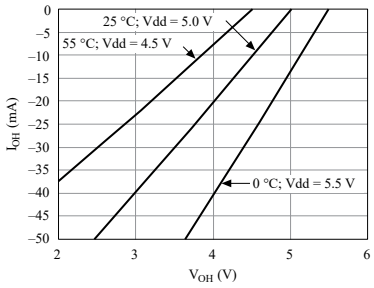


Figure 3. P0.<0..3>: I_{OL} versus V_{OL}

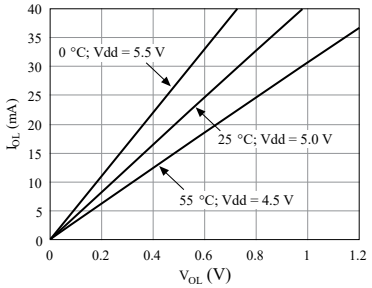
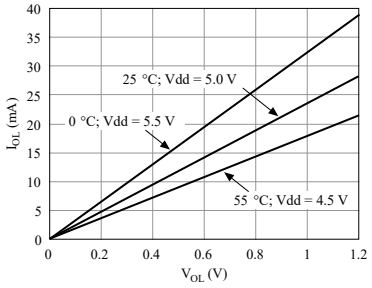


Figure 4. PFI <0..15>/P1/P2: I_{OL} versus V_{OL}



Timing I/O

Number of counter/timers	4
Resolution	32 bits
Counter measurements	Edge counting, pulse, pulse width, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding

Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	100 MHz, 20 MHz, 100 kHz
External base clock frequency	0 MHz to 25 MHz
Base clock accuracy (warranted)	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Routing options for inputs	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR, many internal signals
FIFO	127 samples per counter
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O

Phase-Locked Loop (PLL)

Number of PLLs	1

Table 2. Reference Clock Locking Frequencies

Reference Signal	Locking Input Frequency (MHz)
PXIe_DSTAR<A,B>	10, 20, 100

Reference Signal	Locking Input Frequency (MHz)
PXI_STAR	10, 20
PXIe-CLK100	100
PXI_TRIG <0..7>	10, 20
PFI <0..15>	10, 20

Outside of PLL	100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR
Polarity	Software-selectable for most signals
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Digital waveform generation (DO) function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Digital waveform acquisition (DI) function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Device-to-Device Trigger Bus

Input source	PXI_TRIG <0..7>, PXI_STAR, PXIe-DSTAR<A,B>
Output destination	PXI_TRIG <0..7>, PXIe_DSTARC
Output selections	10 MHz Clock; many internal signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Bus Interface

Form factor	x1 PXI Express peripheral module, specification rev 1.0 compliant
Slot compatibility	x1 and x4 PXI Express or PXI Express hybrid slots
DMA channels	7 DMA, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

Power Requirements

Notice The protection provided by the PXIe-6739 can be impaired if it is used in a manner not described in the user documentation.

+3.3 V	3.0 W
+12 V	20.8 W

Current Limits

Caution Exceeding the current limits may cause unpredictable behavior by the device and/or chassis.

+5 V terminal (connector 0)	1 A maximum [6]
+5 V terminal (connector 1)	1 A maximum [6]
P0/P1/P2/PFI and +5 V terminals combined	1.4 A maximum

Physical

Dimensions (not including connectors)	16 cm x 10 cm (6.3 in. x 3.9 in.)
Weight	173 g (6.1 oz)
I/O connector	2 68-pin VHDCI

Calibration

Recommended warm-up time	15 minutes
Calibration interval	2 years

Safety Voltages

Connect only voltages that are below these limits.

Channel-to-earth ground	±11 V, Measurement Category I

Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.

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Shock and Vibration

Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2

	limits.)
Random vibration	
Operating	5 to 500 Hz, 0.3 g RMS
Nonoperating	5 to 500 Hz, 2.4 g RMS (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Environmental

Maximum altitude	
Pollution degree	

Indoor use only.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

This product meets the requirements of the following environmental standards for electrical equipment for measurement, control, and laboratory use.

Operating Environment

Ambient temperature	0 to 55 °C

range	(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800FClass 3 low temperature limits and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10 to 90% RH, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	to ()
Relative humidity range	()

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

CE Compliance CE

- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)