NI-6589 Getting Started

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NI 6589 Getting Started

Note Before you begin, complete the software and hardware installation instructions in the getting started guide for your FlexRIO FPGA module or Controller for FlexRIO.

The NI 6589 is a FlexRIO adapter module designed to work in conjunction with FlexRIO FPGA modules and Controllers for FlexRIO.

The NI 6589 features 20 LVDS channels (16 data and 4 PFI), and sample rates up to 1 Gbit/s on LVDS channels.

This document explains how to install and configure the NI 6589.

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by NI could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).

Note To ensure the specified EMC performance, you must attach EMI gaskets (NI part number 746228-01) to both sides of your NI 6589 before using.

FlexRIO Documentation

Table 1. FlexRIO Documentation Locations and Descriptions

Document	Location	Description
Getting started guide for your FlexRIO FPGA module or Controller for FlexRIO	Available from the Start menu and at ni.com/manuals.	Contains installation instructions for your FlexRIO system.
Specifications document for your FlexRIO FPGA module or Controller for FlexRIO	Available from the Start menu and at ni.com/manuals.	Contains specifications for your FlexRIO FPGA module or Controller for FlexRIO.
Getting started guide for your adapter module	Available from the Start menu and at ni.com/manuals.	Contains signal information, examples, and CLIP details for your adapter module.
Specifications document for your adapter module	Available from the Start menu and at ni.com/manuals.	Contains specifications for your adapter module.
LabVIEW FPGA Module Help	Embedded in ***LabVIEW Help*** and at ni.com/manuals.	Contains information about the basic functionality of the LabVIEW FPGA Module.
Real-Time Module Help	Embedded in ***LabVIEW Help*** and at ni.com/manuals.	Contains information about real-time programming concepts, step-by-step instructions for using LabVIEW with the Real-Time Module, reference information about Real-Time Module VIs and functions, and information about LabVIEW features on real-time operating systems.
FlexRIO Help	Available from the Start menu and at ni.com/manuals.	Contains information about the FPGA module front panel

Document	Location	Description
		connectors and I/O, controller for FlexRIO front panel connectors and I/O, programming instructions, and adapter module component-level IP (CLIP).
LabVIEW Examples	Available in NI Example Finder. In LabVIEW, click **Help** » **Find Examples** » **Hardware Input and Output** » **FlexRIO**.	Contains examples of how to run FPGA VIs and Host VIs on your device.
IPNet	Located at ni.com/ipnet.	Contains LabVIEW FPGA functions and intellectual property to share.
FlexRIO product page	Located at ni.com/flexrio.	Contains product information and data sheets for FlexRIO devices.

FlexRIO Examples

FlexRIO includes several example applications for LabVIEW. These examples serve as interactive tools, programming models, and as building blocks in your own applications.

Accessing FlexRIO Examples

FlexRIO examples are available in LabVIEW's NI Example Finder. Complete the following steps to access the examples by task.

1. In LabVIEW, click **Help** » **Find Examples**.
2. In the NI Example Finder window that appears, click **Hardware Input and Output** » **FlexRIO**.

   Click on an example and refer to the Information window for a description of the example. Refer the Requirements window for a list of hardware that can run the example.

You can also click the Search tab to search all installed examples by keyword. For example, search for `FlexRIO` to locate all FlexRIO examples.

Online examples are also available to demonstrate FlexRIO basics, such as using DRAM, acquiring data from adapter modules, and performing high throughput streaming. To access these examples, search `FlexRIO examples` in the **Search the community** field at ni.com/examples.

Verifying the System Requirements

To use the NI 6589, your system must meet certain requirements. For more information about minimum system requirements, recommended system, and supported application development environments (ADEs), refer to the readme, which is installed or available at ni.com/manuals.

Unpacking

Caution To prevent ESD from damaging the devices, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.

1. Touch the antistatic package to a metal part of the computer chassis.
2. Remove each module from the package and inspect it for loose components or any other sign of damage.

   Notice Never touch the exposed pins of connectors.

   Note Do not install a device if it appears damaged in any way.
3. Unpack any other items and documentation from the kit.

Store the devices in the antistatic package when they are not in use.

Preparing the Environment

Ensure that the environment you are using the NI 6589 in meets the following

specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	0 °C to 55 °C
Operating humidity (IEC 60068-2-56)	10% to 90% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m at 25 °C ambient temperature

Indoor use only.

Note Refer to the ***NI 6589 Specifications*** at ni.com/manuals for complete specifications.

Caution Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.

Installing the NI 6589

Refer to ***NI FlexRIO FPGA Module Installation Guide and Specifications*** for instructions about how to install your FlexRIO system, including the NI 6589.

Related information:

- NI FlexRIO FPGA Module Installation Guide and Specifications

Cables

Caution You must operate the NI 6589 with shielded cables and shielded accessories to ensure compliance with the EMC requirements defined in the ***NI 6589 Specifications***. Do not use unshielded cables or accessories unless they are installed in a shielded enclosure with properly designed and shielded input/output ports and are connected to the NI 6589 using a shielded cable. If unshielded cables or accessories are not properly installed and shielded, the EMC specifications for the NI 6589 are no longer guaranteed.

Use a shielded 50 Ω coaxial cable with an SMA plug end to connect to the PFI 0 and CLOCK IN connectors on the NI 6589 front panel. Use the NI SHB12X-B12X shielded cable (NI part number 192344-01) or the NI SHB12X-H3X24 differential flying-lead cable (NI part number 196236-1R5) to connect to the DDC connector. You can also connect the NI SMA-2164 accessory to the NI 6589 through the SHB12X-B12X shielded cable for testing and debugging.

Note If you design a custom cabling solution with the DDC connector (779157-01) and SHB12X-B12X shielded cable (192344-01), the NI 6589 pinout is reversed at the end connector. For example, the signal shown on pin 1 maps to pin 73 at the end connector.

The following NI cables and accessories are not properly shielded for EMC-compliant use with the NI 6589:

- NI SMA-2164 accessory
- NI SHB12X-H3X24 differential flying-lead cable

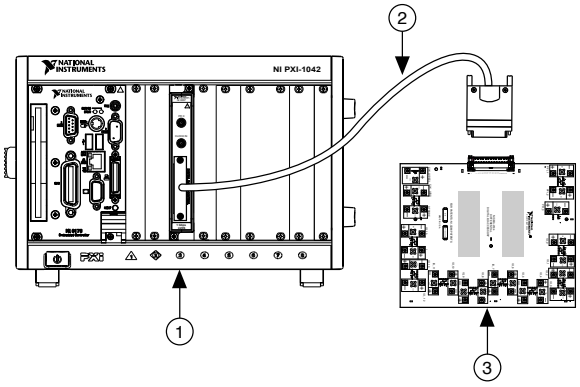
Note Whether you use NI cables and accessories or design your own, terminate cables properly to avoid improper measurements caused by signal reflections, overshoot, and undershoot.

Accessories

The NI SMA-2164 test fixture is a breakout box for differential signals. This fixture provides an easy way to connect to other devices for testing and debugging.

The following figure shows how to connect the differential DDC connector to the NI SMA-2164, using the NI SHB12X-B12X cable. For more information about using the NI SMA-2164, refer to the ***NI SMA-2164/2165 Test Fixture User Guide***.

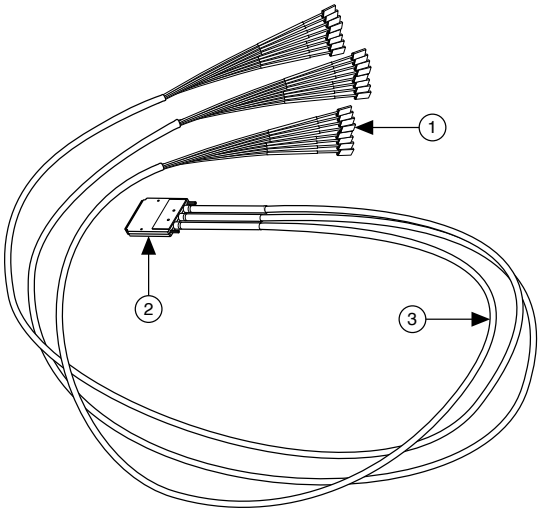
Figure 1. Connecting the NI SMA-2164 Accessory



1. PXI/PXIe Chassis with an NI 6589R
2. NI SHB12-B12X Cable
3. NI SMA-2164

A flying lead cable, the NI SHB12X-H3X24, is also available for differential signals. This cable offers connectivity similar to that found on a typical logic analyzer, so you can use it in logic analyzer-type applications. This cable is shown in the following figure.

Figure 2. NI SHB12X-H3X24 Flying Lead Cable



1. Leads (1 × 3 Header Receptacle)
2. DDC Connector
3. Removeable Sleeving

Custom Accessories

If you are creating a custom accessory to use with a DUT with a VHDCI DDC connector, you can purchase the mating connector for the VHDCI cable from NI. For more information about creating these custom accessories, refer to the ***Interfacing to the NI Digital Waveform Generator/Analyzer using the VHDCI Connector*** application note.

If you are designing a custom accessory to use with a device that uses an InfiniBand connector, you can also purchase this connector from NI.

Visit ***ni.com/info*** and enter the Info Code `rdinwa` to download this note.

Note If you design a custom cabling solution with the DDC connector (779157-01) and SHB12X-B12X shielded cable (192344-01), the NI 6589 pinout is reversed at the end connector. For example, the signal shown on pin 1 maps to pin 73 at the end connector.

For more information about connecting I/O signals on your device, refer to the

NI 6589 Specifications.

Confirming that Measurement & Automation Explorer (MAX) Recognizes the Device

Use Measurement & Automation Explorer (MAX) to configure your NI hardware. MAX informs other programs about which devices reside in the system and how they are configured. MAX is automatically installed with FlexRIO Support.

1. Launch MAX by navigating to **Start** » **All Programs** » **National Instruments** » **NI MAX** or by clicking the NI MAX desktop icon.
2. In the Configuration pane, double-click **Devices and Interfaces** to see the list of installed devices. Installed devices appear under the name of their associated chassis.
3. (PXI and PXI Express devices only) Expand your **Chassis** tree item. MAX lists all devices installed in the chassis. Your default device names may vary.

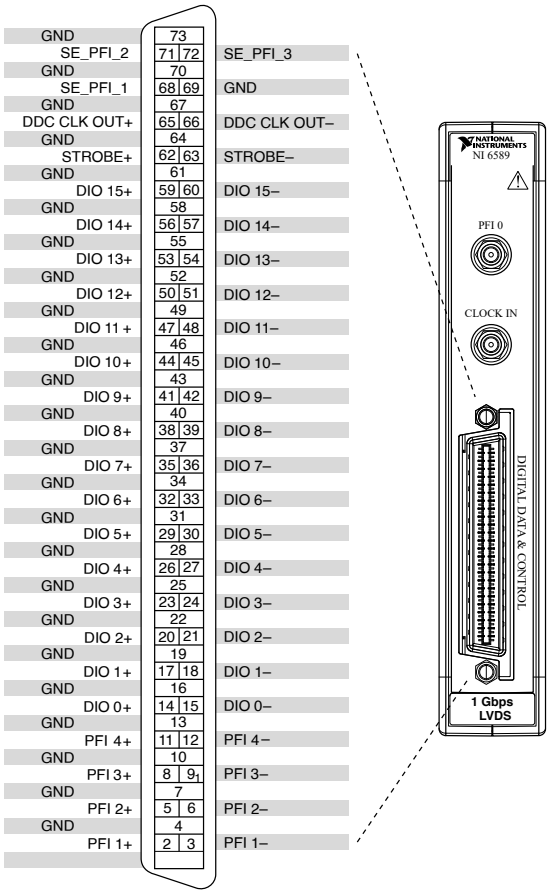
   Note If you do not see your hardware listed, press <F5> to refresh the list of installed devices. If the device is still not listed, power off the system, ensure the device is correctly installed, and restart.

4. (Controllers for FlexRIO only) Your device appears under the **Remote Devices** section.

Front Panel and Connector Pinouts

The NI 6589 provides one PFI signal and one clock signal through the two SMA connectors on the device front panel. Additionally, the NI 6589 provides sixteen LVDS signals, four LVDS PFI signals, three single-ended PFI signals, and an LVDS clock out signal on the Digital Data & Control (DDC) connector. The following figure shows the front panel connector and signal descriptions for the NI 6589.

Figure 3. NI 6589 Front Panel and Connector Pinout



Caution To avoid permanent damage to the NI 6589, disconnect all signals connected to the NI 6589 before powering down the module, and connect signals only after the adapter module has been powered on by the FlexRIO FPGA module or Controller for FlexRIO.

Caution Connections that exceed any of the maximum ratings of any connector on the NI 6589 can damage the device and the chassis. NI is not liable for any damage resulting from such connections.

Note If you design a custom cabling solution with the Infiniband connector (779157-01) and the SHB12X-B12X LVDS shielded cable (192344-01), the NI 6589 pinout is reversed at the end connector. For example, the signal shown on pin 1 maps to pin 73 in the pinout at the end connector.

The following table contains SMA pin location information and signal information for

the NI 6589. The signal names listed in this table refer to the signals shown in the front panel pinout.

Table 2. SMA Connector Names and Descriptions

Signal Name	Connector	Signal Type	Signal Description
PFI 0	PFI 0	Control	Bidirectional single-ended terminal for channel PFI 0.
CLOCK IN	CLOCK IN	Clock	External single-ended clock input terminal.

The following table contains DDC pin location information for the NI 6589. The signal names listed in this table refer to the signals shown in the front panel pinout.

Table 3. NI 6589 DDC Connector Names and Descriptions

Signal Name	Pin(s)	Signal Type	Signal Description
DDC CLK OUT+	65	Control	Positive terminal for the LVDS exported Sample Clock.
DDC CLK OUT-	66	Control	Negative terminal for the LVDS exported Sample Clock.
STROBE+	62	Control	Positive differential terminal for the external Sample Clock source that can be used for synchronous dynamic acquisition.
STROBE-	63	Control	Negative differential terminal for the external Sample Clock source that can be used for synchronous dynamic acquisition.
DIO<0..15>+	14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53, 56, 59	Data	Positive differential terminal for the bidirectional digitial

Signal Name	Pin(s)	Signal Type	Signal Description
			I/O data channels 0 through 15.
DIO<0..15>-	15, 18, 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 57, 60	Data	Negative differential terminal for the bidirectional digitial I/O data channels 0 through 15.
PFI <1..4>+	2, 5, 8, 11	Control	Positive differential terminals for bidirectional PFI channels 1 through 4.
PFI <1..4>-	3, 6, 9, 12	Control	Negative differential terminals for bidirectional PFI channels 1 through 4.
SE_PFI<1..3>	68, 71, 72	Control	Single-ended terminals for bidirectional PFI channels 1 through 3.
GND	1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 42, 46, 49, 52, 55, 58, 69	Ground	Ground reference for signals.

Related information:

- For more information about NI 6589 front panel connectors, refer to the NI 6589 Specifications at ni.com/manuals.

Block Diagrams

The following figures show the data flow through the NI 6589. Single-ended data lines use standard clock levels to interpret data as either a binary zero or a one in high-speed digital data transfers. Differential data lines provide a low-noise, low-power, low-amplitude differential method for high-speed digital data transfer.

Figure 4. Clock Input Signal

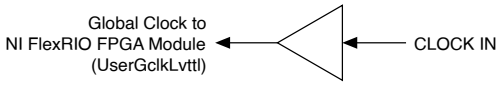


Figure 5. LVDS Data and PFI Lines

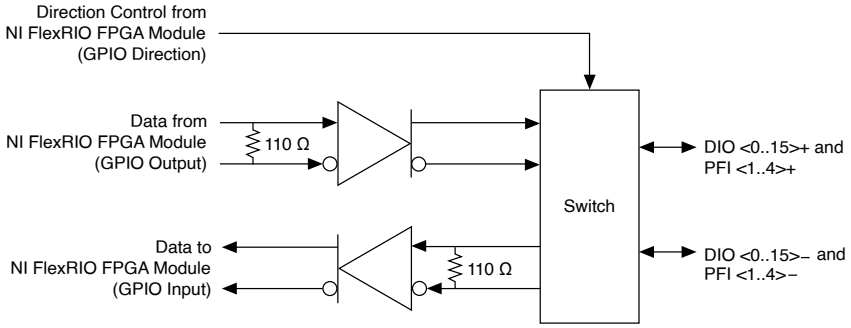


Figure 6. Single-Ended PFI Lines

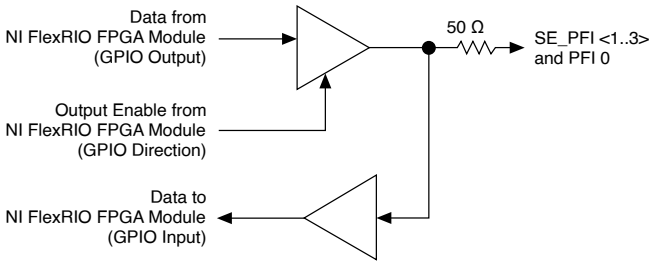


Figure 7. Clock Output Signals

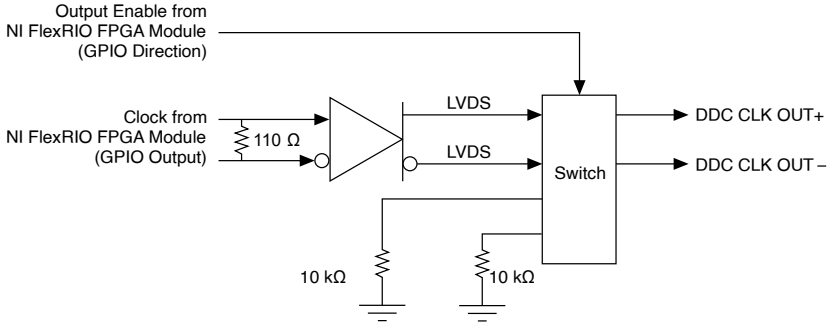
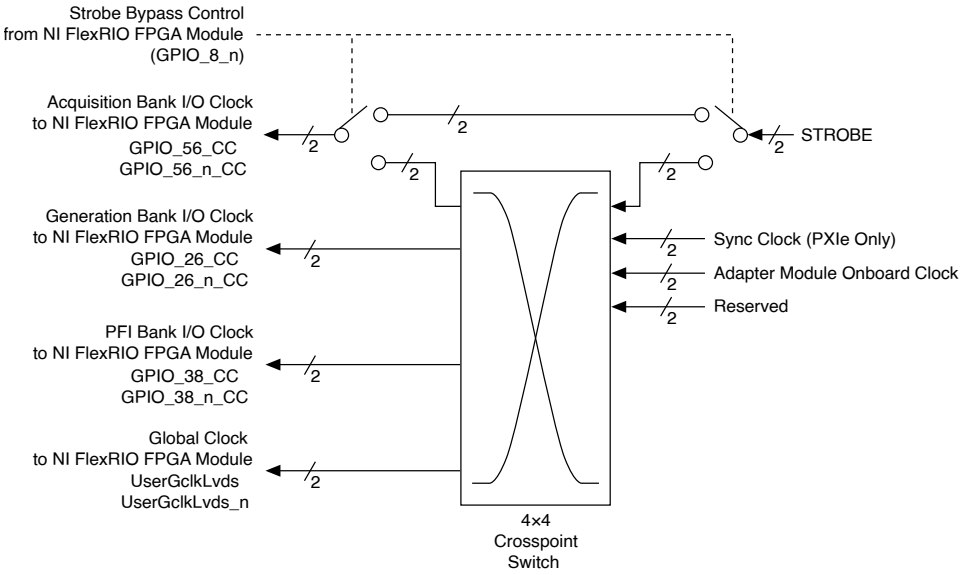


Figure 8. Crosspoint Switch



Related concepts:

- Component-Level Intellectual Property (CLIP)

Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. FlexRIO devices support two types of CLIP: user-defined and socketed.

- ***User-defined CLIP*** allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- ***Socketed CLIP*** provides the same IP integration of the user-defined CLIP, but it also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The NI 6589 ships with socketed CLIP items that add module I/O to the LabVIEW project.

Related reference:

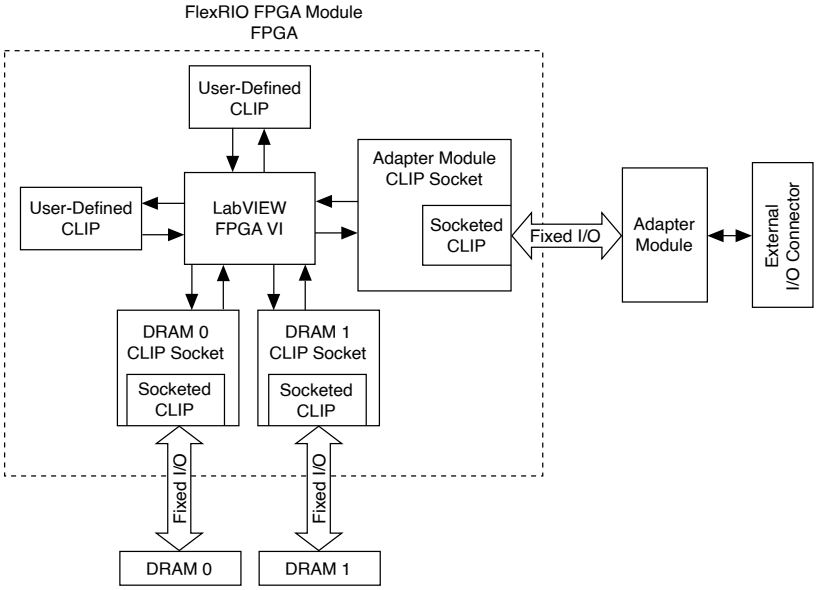
- Block Diagrams

CLIP and LabVIEW FPGA

The interface between the NI 6589 CLIP and LabVIEW FPGA in the following figures.

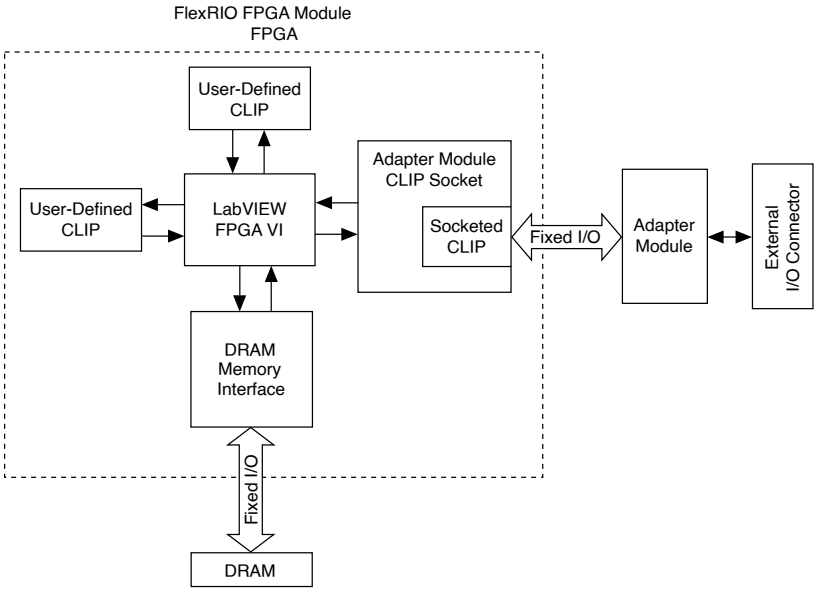
If you are using a FlexRIO FPGA module with a Virtex-5 FPGA, refer to the following figure, which shows the relationship between the CLIP and an FPGA VI configured for use with a Virtex-5 FPGA target.

Figure 9. CLIP and FPGA VI Relationship (Virtex-5)



If you are using a FlexRIO FPGA module or Controller for FlexRIO with a Kintex-7 FPGA, refer to the following figure, which shows the relationship between the CLIP and an FPGA VI configured for use with a Kintex-7 FPGA target.

Figure 10. CLIP and FPGA VI Relationship (Kintex-7)



NI 6589 CLIP

The NI 6587 ships with socketed CLIP that adds module I/O to the LabVIEW project. The NI-developed are as follows:

Note All NI 6589 CLIP items allow individual clock output inversion.

- **NI 6589 Basic Connector CLIP**—

  Provides read/write access to all low-voltage differential signal (LVDS) and single-ended channels, where the channels are grouped by connector. You can access the LVDS data and direction lines using a U16 data type in which each bit position corresponds to an individual channel. You can access the LVDS PFI lines and the single-ended PFI lines using a Boolean control.

  This CLIP provides access to the following signals.

  - Sixteen bidirectional data LVDS lines
  - Four LVDS PFI lines
  - One LVDS STROBE line
  - One LVDS clock output signal
  - Four single-ended PFI lines
  - One single-ended clock input signal

- **NI 6589 Serdes Channel CLIP**—

  Provides read/write access to all LVDS and single-ended channels using a channel-based interface. You can access the LVDS data and PFI channels using a U16 data type in which the top six bits are unused. Each LVDS line, PFI line, and clock output is connected to an OSERDES or ISERDES block that serializes or deserializes, respectively, the signal by a factor of 10 by default. During acquisition, the NI 6589 reads or writes ten bits of data per channel to or from the ISERDES or OSERDES blocks. All OSERDES and ISERDES blocks are set to double data rate (DDR) mode. The SERDES will serialize or deserialize the LVDS data in bit order from MSB to LSB.

  This CLIP provides access to the following signals.

  - Sixteen bidirectional data LVDS lines
  - Four LVDS PFI lines
  - One LVDS STROBE line
  - One LVDS clock output signal
  - Four single-ended PFI lines
  - One single-ended clock input signal
- **NI 6589 Serdes Connector CLIP**—

  Provides read/write access to all LVDS and single-ended channels, where the channels are grouped by connector. This CLIP conveys parallel data at high speeds. You can access the LVDS data and direction lines using a U16 data type, you can access the LVDS PFI lines using a U8 data type, and you can access the single-ended PFI lines using a Boolean control. In the U8 data type, the top four bits are unused. Each LVDS line, PFI line, and clock output is connected to an OSERDES or ISERDES block that serializes or deserializes, respectively, the signal by a factor of six by default. Therefore, with every regional clock cycle, the NI 6589 reads or writes six samples to or from the ISERDES or OSERDES blocks. All OSERDES and ISERDES blocks are set to double data rate (DDR) mode. The SERDES will serialize or deserialize the LVDS data in bit order from MSB to LSB.

  This CLIP provides access to the following signals.

  - Sixteen bidirectional data LVDS lines
  - Four LVDS PFI lines
  - One LVDS STROBE line

- One LVDS clock output signal
- Four single-ended PFI lines
- One single-ended clock input signal

The following table lists the NI 6589 SMA connector signals and corresponding FlexRIO FPGA module signals necessary for designing custom component-level IP (CLIP).

Table 4. NI 6589 SMA Signals and FlexRIO FPGA Module Signals

NI 6589	**FlexRIO FPGA Module**		
Signal Name	**GPIO Input**	**GPIO Output**	**GPIO Direction**
PFI 0	GPIO_2_n	GPIO_5_n	GPIO_6_n (as enable)
CLOCK IN	GClk_SE	—	—

The following table lists the NI 6589 DDC connector signals and corresponding FlexRIO FPGA module signals necessary for designing custom component-level IP (CLIP). The ***_CC*** suffix on signals identifies channels that can receive a regional clock.

Table 5. NI 6589 DDC Signals and FlexRIO FPGA Module Signals

NI 6589	**FlexRIO FPGA Module**		
Signal Name	**GPIO Input**	**GPIO Output**	**GPIO Direction**
PFI 1+	GPIO_39_CC	GPIO_36	GPIO_14
PFI 1-	GPIO_39_n_CC	GPIO_36_n	
PFI 2+	GPIO_40_CC	GPIO_41	GPIO_14_n
PFI 2-	GPIO_40_n_CC	GPIO_41_n	
PFI 3+	GPIO_45	GPIO_46	GPIO_15
PFI 3-	GPIO_45 _n	GPIO_46_n	
PFI 4+	GPIO_47	GPIO_48	GPIO_15_n
PFI 4-	GPIO_47_n	GPIO_48_n	
DIO 0+	GPIO_62	GPIO_32	GPIO_4_n
DIO 0-	GPIO_62_n	GPIO_32_n	
DIO 1+	GPIO_63	GPIO_28	GPIO_11

NI 6589	FlexRIO FPGA Module		
Signal Name	**GPIO Input**	**GPIO Output**	**GPIO Direction**
DIO 1-	GPIO_63_n	GPIO_28_n	
DIO 2+	GPIO_64	GPIO_23	GPIO_9_n
DIO 2-	GPIO_64_n	GPIO_23_n	
DIO 3+	GPIO_65	GPIO_19	GPIO_3
DIO 3-	GPIO_65_n	GPIO_19_n	
DIO 4+	GPIO_60	GPIO_31	GPIO_4
DIO 4-	GPIO_60_n	GPIO_31_n	
DIO 5+	GPIO_61	GPIO_27	GPIO_5
DIO 5-	GPIO_61_n	GPIO_27_n	
DIO 6+	GPIO_55	GPIO_22	GPIO_6
DIO 6-	GPIO_55_n	GPIO_22_n	
DIO 7+	GPIO_54	GPIO_18	GPIO_7
DIO 7-	GPIO_54_n	GPIO_18_n	
DIO 8+	GPIO_53	GPIO_30	GPIO_8
DIO 8-	GPIO_53_n	GPIO_30_n	
DIO 9+	GPIO_52	GPIO_25	GPIO_9
DIO 9-	GPIO_52_n	GPIO_25_n	
DIO 10+	GPIO_51	GPIO_21	GPIO_10
DIO 10-	GPIO_51_n	GPIO_21_n	
DIO 11+	GPIO_50	GPIO_17	GPIO_2
DIO 11-	GPIO_50_n	GPIO_17_n	
DIO 12+	GPIO_49_CC	GPIO_29	GPIO_12
DIO 12-	GPIO_49_n_CC	GPIO_29_n	
DIO 13+	GPIO_57_CC	GPIO_24	GPIO_13
DIO 13-	GPIO_57_n_CC	GPIO_24_n	
DIO 14+	GPIO_58_CC	GPIO_20	GPIO_3_n

NI 6589	FlexRIO FPGA Module		
Signal Name	**GPIO Input**	**GPIO Output**	**GPIO Direction**
DIO 14-	GPIO_58_n_CC	GPIO_20_n	
DIO 15+	GPIO_59_CC	GPIO_16	GPIO_1_n
DIO 15-	GPIO_59_n_CC	GPIO_16_n	
STROBE+	GPIO_56_CC	—	GPIO_8_n
	GPIO_26_CC		
	GPIO_38_CC		
	GPIO_LVDS		
STROBE-	GPIO_56_n_CC		
	GPIO_26_n_CC		
	GPIO_38_CC		
	GPIO_LVDS_n		
DDC CLOCK OUT LVDS+	—	GPIO_43	GPIO_7_n (as enable)
DDC CLOCK OUT LVDS-		GPIO_43_n	
SE_PFI_1	GPIO_44_n	GPIO_37_n	GPIO_44 (as enable)
SE_PFI_2	GPIO_42_n	GPIO_34_n	GPIO_42 (as enable)
SE_PFI_3	GPIO_35	GPIO_33_n	GPIO_35_n (as enable)

Related information:

- Refer to the FlexRIO Help for more information about FlexRIO CLIP items, how to configure the NI 6589 with a socketed CLIP, and for a list of available socketed CLIP signals.

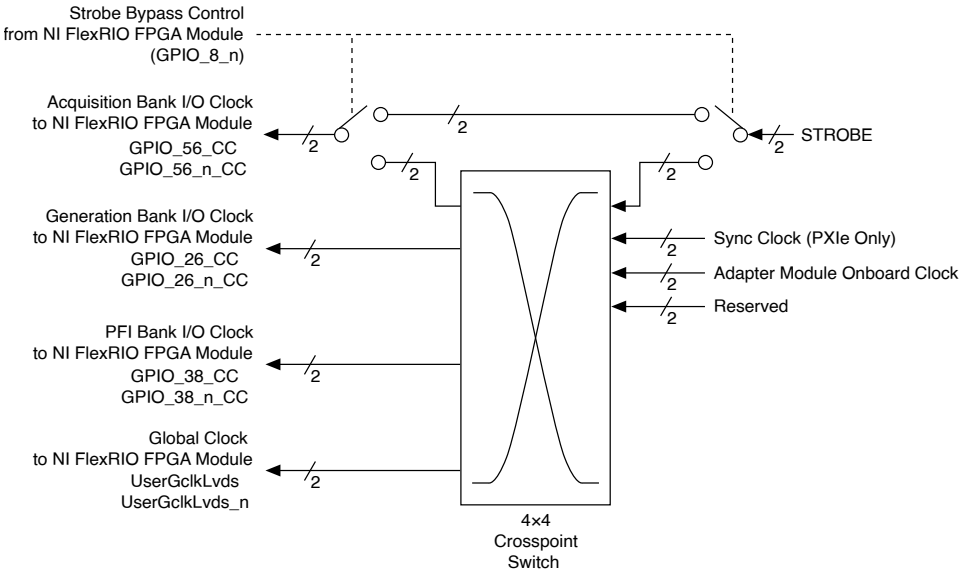
Clocking

The clocks on the NI 6589 control the sample rate and other timing functions on your FlexRIO system. The following figure shows the NI 6589 clock sources routed through the crosspoint switch. The Generation Bank I/O clock, PFI Bank I/O clock, and Global clock are all sourced by the crosspoint switch. The Acquisition Bank I/O clock can be

sourced from the crosspoint switch or accessed directly through the Strobe Bypass path.

Note Only the Acq_IO_Clock_Source signal can use the STROBE Bypass path. If Acq_IO_Clock_Source is set to Strobe Bypass, then Gen_IO_Clock_Source, PFI_IO_Clock_Source, and IO_Module_Clock_1_Source cannot be set to Strobe From Crosspoint Switch.

Figure 11. Crosspoint Switch



In software, each clock output terminal is accessed with a U8 data type. The following table shows the values of the crosspoint switch clock options.

Table 6. Clock Values

Value	Clock Option
0	**Tristate**—Output disabled (high impedance).
2	**Sync Clock (PXI Express Only)**—Clock from PXI Express backplane. You can select **PXI_CLK10** or **DStarA** in the Details category of the IO Module Properties dialog box.
3	**Adapter Module Onboard Clock**—Clock generated from the Si570 clock chip.
4	**Strobe From Crosspoint Switch**—LVDS STROBE signal from crosspoint switch. Use this setting to

Value	Clock Option
	route the LVDS STROBE signal to multiple I/O clocks.
5	**Strobe Bypass**—LVDS STROBE bypasses the crosspoint switch. The propagation delay of the **Strobe Bypass** exactly matches the propagation delay of the data channels. This setting is ideal for source- synchronous applications.

Related information:

- For more information about clock sources, refer to the FlexRIO Help.