PCI-5412 Specifications

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Contents

PCI-5412 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are ***Nominal*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 0 °C to 55 °C
- Interpolation set to maximum allowed factor for a given sample rate
- Signals terminated with 50 Ω
- Low-gain amplifier path set to 2 Vpk-pk
- High-gain amplifier path set to 12 Vpk-pk
- Sample Clock set to 100 MS/s

Typical specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 23 °C±5 °C

CH 0 Analog Output

Number of channels	1
Connector type	SMB jack

Output Voltage

Full-scale voltage		
Main output path[1]	12.00 V pk-pk to 5.64 mV pk-pk into a 50 Ω load	
DAC resolution		14 bits
Maximum output voltage[2]		
Low-gain amplifier path		
50 Ω load	±1.000 Vpk	
1 kΩ load	±1.905 Vpk	
Open load	±2.000 Vpk	
High-gain amplifier path		
50 Ω load	±6.000 Vpk	
1 kΩ load	±11.43 Vpk	

Open load	±12.00 Vpk

Amplitude and Offset

Amplitude range[3], low-gain amplifier path	
Amplitude range[3], high-gain amplifier path	
Amplitude resolution	<0.06% (0.004 dB) of ***Amplitude Range***
Offset range	Span of ±25% of ***Amplitude Range*** with increments <0.0014% of ***Amplitude Range***

Accuracy

DC accuracy (calibrated for high-impedance load)[4]	
Within ±10 °C of self-calibration temperature	±0.2% of amplitude range ±0.05% of offset ±500 µV
0 °C to 55 °C	±0.4% of amplitude range ±0.05% of offset ±1 mV
AC amplitude accuracy[5]	(+2.0% + 1 mV), (-1.0% - 1 mV) (+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical

Output

Output	Software-selectable: 50 Ω or 75 Ω, nominal

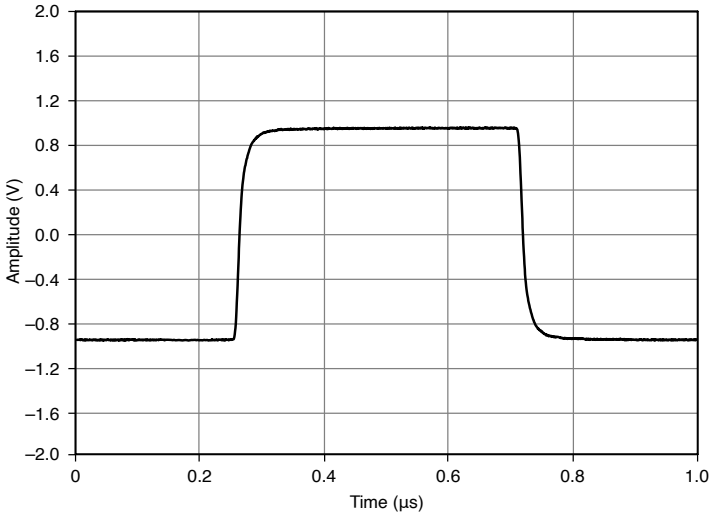
impedance	
Output coupling	DC
Output enable	Software-selectable[6]
Maximum output overload	The CH 0 output can be connected to a 50 Ω, ±12 V source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.
Waveform summing	Supported[7]

Frequency and Transient Response

Bandwidth[8]	20 MHz
Digital interpolation filter[9]	Software-selectable: Finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.
Passband flatness[10]	±1.0 dB from DC to 6 MHz
Pulse response[11]	
Low-gain amplifier path	

Rise/fall time	<20 ns, typical
Aberration	<5%, typical
High-gain amplifier path	
Rise/fall time	<20 ns, typical
Aberration	<5%, typical

Figure 1. Pulse Response, Low-Gain Amplifier Path 50 Ω Load



Suggested Maximum Frequencies for Common Functions

Suggested maximum frequencies[12]	
Low-gain amplifier path	
Sine	20 MHz
Square	5 MHz

Ramp	1 MHz
Triangle	1 MHz
High-gain amplifier path	
Sine	20 MHz
Square	5 MHz
Ramp	1 MHz
Triangle	1 MHz

Spectral Characteristics

Spurious-free dynamic range (SFDR)[13] without harmonics[14]	
Low-gain amplifier path	
1 MHz	70 dB, typical
10 MHz	65 dB, typical
20 MHz	60 dB, typical
High-gain amplifier path	
1 MHz	70 dB, typical

10 MHz	65 dB, typical
20 MHz	60 dB, typical
Total harmonic distortion (THD)[15] (0 °C to 40 °C)	
Low-gain amplifier path	
1 MHz	-59 dBc, typical
10 MHz	-52 dBc, typical
20 MHz	-45 dBc, typical
High-gain amplifier path	
1 MHz	-51 dBc, typical
10 MHz	-40 dBc, typical
20 MHz	-37 dBc, typical
Average noise density[16]	
Low-gain amplifier path	
2 Vpk-pk, 10 dBm amplitude range	45 $\frac{nV}{\sqrt{Hz}}$, -134 dBm/Hz, -144 dBFS/Hz, typical
High-gain amplifier path	

12 Vpk-pk, 25.6 dBm amplitude range	251 $\frac{nV}{\sqrt{Hz}}$, -119 dBm/Hz, -145 dBFS/Hz, typical

Sample Clock

External	CLK IN (SMB front panel connector) External, RTSI<0..7>

Sample Rate Range and Resolution

Sample rate range	
Divide-by-N	23.84 S/s to 100 MS/s
High-Resolution	10 S/s to 100 MS/s
CLK IN	200 kS/s to 105 MS/s
RTSI<0..7>	10 S/s to 20 MS/s
Sample rate resolution	
Divide-by-N	Configurable to (100 MS/s)/N(1 ≤ N ≤ 4,194,304)
High-Resolution	1.06 µHz

CLK IN and RTSI<0..7>	Resolution determined by External Clock source. External Sample Clock duty cycle tolerance 40% to 60%.

Effective Sample Rate

(Interpolation factor) * (Sample rate) = Effective sample rate		
Interpolation factor	**Sample rate**	**Effective sample rate**
1 (Off)	10 S/s to 105 MS/s	10 S/s to 105 MS/s
2	12.5 MS/s to 105 MS/s	25 MS/s to 210 MS/s
4	10 MS/s to 100 MS/s	40 MS/s to 400 MS/s
8	10 MS/s to 50 MS/s	80 MS/s to 400 MS/s

Sample Clock Delay Range and Resolution

Delay adjustment range	
Divide-by-N	±1 Sample Clock period
High-Resolution	±1 Sample Clock period
Delay adjustment resolution	
Divide-by-N	<10 ps
High-Resolution	Sample Clock period/16,384

System Phase Noise Jitter (10 MHz Carrier)

System phase noise density offset[17]	
100 Hz	-90 dBc/Hz, typical
1 kHz	-110 dBc/Hz, typical
10 kHz	-120 dBc/Hz, typical
System output jitter (integrated from 100 Hz to 100 kHz)[17]	<7 ps rms, typical
External Sample Clock input jitter tolerance	
Cycle-cycle jitter	±300 ps, typical
Period jitter	±1 ns, typical

Exported Sample Clock Destinations

Destinations[18]	PFI <0..1> (SMB front panel connectors) RTSI<0..6>
Maximum frequency	
PFI <0..1>	105 MHz
RTSI<0..6>	20 MHz

Duty cycle	
PFI <0..1>	25% to 65%

Onboard Clock (Internal VCXO)

Source	Internal Sample Clocks can either be locked to a Reference Clock using a phase-locked loop or derived from the onboard VCXO frequency reference.
Frequency accuracy	±25 ppm

Phase-Locked Loop (PLL) Reference Clock

Sources[19]	RTSI_7 (RTSI_CLK) CLK IN (SMB front panel connector)
Frequency accuracy	When using the PLL, the frequency accuracy of the PCI-5412 is solely dependent on the frequency accuracy of the PLL Reference Clock source.
Lock time	≤200 ms
Frequency range[20]	5 MHz to 20 MHz in increments of 1 MHz[21]
Duty cycle range	40% to 60%

Destinations	PFI <0..1> (SMB front panel connectors) RTSI<0..6>

CLK IN

Connector type	SMB jack
Direction	Input
Destinations	Sample Clock PLL Reference Clock

Frequency range	
Sample Clock destination and sine waves	1 MHz to 105 MHz
Sample Clock destination and square waves	200 kHz to 105 MHz
PLL Reference Clock destination	5 MHz to 20 MHz

Input voltage range into 50 Ω	
Sine wave	0.65 V pk-pk to 2.8 V pk-pk (0 dBm to +13 dBm)
Square wave	0.2 V pk-pk to 2.8 V pk-pk

Maximum input overload	±10 V

Input impedance	50 Ω
Input coupling	AC

PFI 0 and PFI 1

Connector type	SMB jack (x2)
Direction	Bidirectional
Frequency range	DC to 105 MHz
As an input (trigger)	
Destinations	Start Trigger
Maximum input overload	-2 V to +7 V
V IH	2.0 V
V IL	0.8 V
Input impedance	1 kΩ
As an output (event)	
Sources	Sample Clock divided by integer K (1 ≤ K ≤ 4,194,304)

	Sample Clock Timebase (100 MHz) divided by integer M (2 ≤ M ≤ 4,194,304) PLL Reference Clock Marker Exported Start Trigger (Out Start Trigger)
Output impedance	50 Ω
Maximum output overload	-2 V to +7 V
Minimum V OH[22]	
Open load	2.9 V
50 Ω load	1.4 V
Maximum V OL[22]	
Open load	0.2 V
50 Ω load	0.2 V
Rise/fall time (20% to 80%)[23]	≤2.0 ns

Start Trigger

Sources	PFI<0..1> (SMB front panel connectors) RTSI<0..7> Software (use node or function call) Immediate (does not wait for a trigger). The default is Immediate.
Modes	Single Continuous Stepped Burst
Edge detection	Rising
Minimum pulse width	25 ns

Delay from Start Trigger to CH 0 analog output	
Digital interpolation filter disabled	43 Sample Clock periods + 110 ns, typical
Interpolation factor of 2	57 Sample Clock periods + 110 ns, typical
Interpolation factor of 4	63 Sample Clock periods + 110 ns, typical
Interpolation factor of 8	64 Sample Clock periods + 110 ns, typical

Destinations	A signal used as a trigger can be routed out to any destination listed in the ***Destinations*** specification of the Markers section
Exported trigger delay	65 ns, typical
Exported trigger pulse width	>150 ns

Markers

Destinations	PFI <0..1> (SMB front panel connectors) RTSI<0..6>
Quantity	One marker per segment
Quantum	Marker position must be placed at an integer multiple of four samples.
Width	>150 ns

Skew	
RTSI<0..6>	
With respect to analog output	±2 Sample Clock periods

Arbitrary Waveform Generation Mode

Memory usage	The PCI-5412 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters—such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage—are flexible and user-defined.

Onboard memory size	
8 MB standard	8,388,608 bytes
32 MB option	33,554,432 bytes
256 MB option	268,435,456 bytes

Output modes	Arbitrary waveform[24] Arbitrary sequence[25]

Minimum waveform size	
Arbitrary waveform mode	
Single Trigger mode	16 samples
Continuous Trigger mode	16 samples
Stepped Trigger mode	32 samples
Burst Trigger mode	16 samples
Arbitrary sequence mode	

Single Trigger mode	16 samples
Continuous Trigger mode	96 samples at >50 MS/s 32 samples at ≤50 MS/s
Stepped Trigger mode	96 samples at >50 MS/s 32 samples at ≤50 MS/s
Burst Trigger mode	512 samples at >50 MS/s 256 samples at ≤50 MS/s
Loop count	1 to 16,777,215 Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of four samples.

Memory Limits[26]

Maximum waveform memory, arbitrary waveform mode	
8 MB standard	4,194,176 samples
32 MB option	16,777,088 samples
256 MB option	134,217,600 samples

Maximum waveform memory, arbitrary sequence mode[27]	
8 MB standard	4,194,120 samples
32 MB option	16,777,008 samples
256 MB option	134,217,520 samples
Maximum waveforms, arbitrary sequence mode[27]	
8 MB standard	65,000 Burst trigger: 8,000
32 MB option	262,000 Burst trigger: 32,000
256 MB option	2,097,000 Burst trigger: 262,000
Maximum segments in a sequence, arbitrary sequence mode	
8 MB standard	104,000 Burst trigger: 65,000
32 MB option	418,000 Burst trigger: 262,000

256 MB option	3,354,000 Burst trigger: 2,090,000

Calibration

Self-calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.
External calibration	External calibration calibrates the VCXO, voltage reference, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.
Calibration interval	Specifications valid within two years of external calibration.
Warm-up time	15 minutes

Power

Total power	
Normal operation	22 W, typical
Overload operation[28]	26 W, typical

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-25 °C to 85 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Storage shock	50 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)

Nonoperating random vibration	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Physical

Dimensions	34.1 cm × 2.0 cm × 10.7 cm (13.4 in. × 0.8 in. × 4.2 in.)
Weight	480 g (17 oz)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions

- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)