# PXI-5122 Specifications

2025-03-10

# Contents

# PXI-5122 Specifications

## Definitions

***Warranted*** specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

***Characteristics*** describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Typical*** unless otherwise noted.

## Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 100 MS/s

## PXI-5122 Pinout

Use the pinout to connect to terminals on the PXI-5122.

### Connectors

The PXI-5122 has the following six connectors on the front panel.

| Connector | Description | Function |
|---|---|---|
| CH 0, CH 1 | Standard BNC connector | Analog input connection; digitizes data and triggers acquisitions |
| TRIG | Standard BNC connector | External analog trigger connection; signals on the TRIG connector cannot be digitized |
| CLK IN | SMB jack | Imports an external reference or sample clock to the digitizer |
| CLK OUT | SMB jack | Exports the digitizer reference or sample clock |
| AUX I/O | 9-pin mini-circular DIN connector | Provides access to the external digital trigger lines, PFI 0 and PFI 1 (with optional cable) |

## PXI-5122 AUX I/O Connector Pin Assignments

PFI 0 and PFI 1 are accessible through the 9-pin connector (AUX I/O), shown in the following figure.

Figure 1. 9-Pin DIN Connector

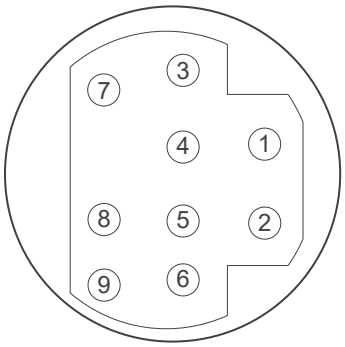



Table 1. Pin Assignments and Connector Descriptions

| Pin Number | Description |
|---|---|
| 1 | 5 V (Fused) |
| 2 | GND |
| 3 | Reserved |
| 4 | Reserved |
| 5 | Reserved |
| 6 | PFI 1 |
| 7 | Reserved |

| Pin Number | Description |
|---|---|
| 8 | Reserved |
| 9 | PFI 0 |

**Note** Be sure to use an NI adapter cable or a cable that has the same pinout shown in the previous figure.

# Vertical

## Analog Input

| | |
|---|---|
| Number of channels | Two (simultaneously sampled) |
| Connectors | BNC |

## Impedance and Coupling

| | |
|---|---|
| Input impedance (software-selectable) | 50 Ω ± 2.0%<br><br>1 MΩ ± 0.75% in parallel with a nominal capacitance of 29 pF |
| Input coupling (software-selectable) | AC[1]<br><br>DC<br><br>GND |

1. AC coupling available on 1 MΩ input only.

# Voltage Levels

Table 2. Full Scale (FS) Input Range and Programmable Vertical Offset

| Range ($V_{pk-pk}$) | Vertical Offset Range | |
|---|---|---|
| | 50 Ω Input | 1 MΩ Input |
| 0.2 V | ±0.1 V | |
| 0.4 V | ±0.2 V | |
| 1 V | ±0.5 V | |
| 2 V | ±1 V | |
| 4 V | ±2 V | |
| 10 V | — | ±5 V |
| 20 V (1 MΩ only) | — | — |

| Maximum input overload | |
|---|---|
| 50 Ω | 7 $V_{rms}$ with \|Peaks\| ≤10 V |
| 1 MΩ | \|Peaks\| ≤42 V |

# Accuracy

| | |
|---|---|
| Resolution | 14 bits |

Table 3. DC Accuracy[2], Warranted

| Input Range ($V_{pk-pk}$) | DC Accuracy |
|---|---|
| 0.2 V and 0.4 V | ±(0.65% of input + 1.0 mV) |
| 1 V | ±(0.65% of input + 1.2 mV) |
| 2 V | ±(0.65% of input + 1.6 mV) |

2. Programmable vertical offset = 0 V. Within ±5 °C of self-calibration temperature.

| Input Range ($V_{pk-pk}$) | DC Accuracy |
|---|---|
| 4 V and 10 V | ±(0.65% of input + 8.0 mV) |
| 20 V (1 MΩ only) | ±(0.65% of input + 13.0 mV) |

| | |
|---|---|
| Programmable vertical offset accuracy[3][3] | ±0.4% of offset setting, Warranted |

Table 4. DC Drift, nominal

| Input Range ($V_{pk-pk}$) | 50 Ω and 1 MΩ |
|---|---|
| 0.2 V, 0.4 V, 1 V, and 2 V | ±(0.057% of input + 0.006% of FS + 100 µV) per °C |
| 4 V, 10 V | ±(0.057% of input + 0.006% of FS + 900 µV) per °C |
| 20 V (1 MΩ only) | |

| **AC amplitude accuracy**[3] | |
|---|---|
| 50 Ω | ±0.06 dB (±0.7%) at 50 kHz |
| 1 MΩ | ±0.09 dB (±1.0%) at 50 kHz |
| Crosstalk[4] | ≤-100 dB at 10 MHz |

## Bandwidth and Transient Response

| **Bandwidth (±3 dB)**[5] | |
|---|---|
| 0.2 V input range | 80 MHz up to 40 °C,[6] warranted |

3. Within ±5 °C of self-calibration temperature.
4. CH 0 to/from CH 1 and External Trigger to CH 0 or CH 1.
5. Filters off.

| | |
|---|---|
| All other input ranges | 100 MHz, warranted |
| **Rise/fall time** | |
| 0.2 V input range | 4.2 ns |
| All other input ranges | 3.5 ns |
| **Bandwidth limit filters**[7] | |
| Noise filter (2-pole Bessel) | 20 MHz |
| Anti-alias filter (6-pole Chebyshev) | 40 MHz (-6 dB)<br>35 MHz (±3 dB), warranted |
| AC coupling cutoff (-3 dB)[8] | 12 Hz |

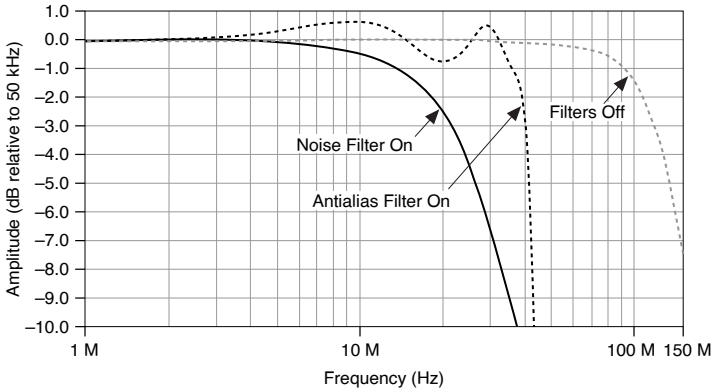
Table 5. Passband Flatness[9]

| Filter Settings | Input Range ($V_{pk-pk}$) | 50 Ω and 1 MΩ |
|---|---|---|
| Filters off | 0.2 V | ±0.4 dB (DC to 20 MHz)<br>±1 dB (20 MHz to 40 MHz) |
| | All other input ranges | ±0.4 dB (DC to 20 MHz)<br>±1.0 dB (20 MHz to 50 MHz) |

6. 78 MHz above 40 °C.
7. Only one filter can be enabled at any given time. The anti-alias filter is enabled by default.
8. AC coupling available on 1 MΩ input only.
9. Referenced to 50 kHz.

| Filter Settings | Input Range ($V_{pk-pk}$) | 50 Ω and 1 MΩ |
|---|---|---|
| Anti-alias filter on | All ranges | ±1.2 dB (DC to 16 MHz)<br>±1.6 dB (16 MHz to 32 MHz) |

Figure 2. PXI-5122 Frequency Response, Measured




# Spectral Characteristics

Table 6. Spurious-Free Dynamic Range with Harmonics (SFDR)[10]

| Range ($V_{pk-pk}$) | 50 Ω | 1 MΩ |
|---|---|---|
| 0.2 V | 75 dBc | 70 dBc |
| 0.4 V | 75 dBc | 70 dBc |
| 1 V | 75 dBc | 70 dBc |
| 2 V | 75 dBc | 70 dBc |
| 4 V | 65 dBc | 70 dBc |
| 10 V | 65 dBc | 60 dBc |
| 20 V | — | 60 dBc |

10. 10 MHz, -1 dBFS input signal. Includes the 2nd through the 5th harmonics. Measured from DC to 50 MHz.

Table 7. Total Harmonic Distortion (THD)[11]

| Range ($V_{pk-pk}$) | 50 Ω | 1 MΩ |
|---|---|---|
| 0.2 V | -75 dBc | -68 dBc |
| 0.4 V | -75 dBc | -68 dBc |
| 1 V | -75 dBc | -68 dBc |
| 2 V | -73 dBc | -68 dBc |
| 4 V | -63 dBc | -68 dBc |
| 10 V | -63 dBc | -58 dBc |
| 20 V | — | -58 dBc |

| | |
|---|---|
| Intermodulation distortion[12] | -75 dBc |

Table 8. Signal-to-Noise Ratio (SNR)[13]

| Range ($V_{pk-pk}$) | 50 Ω | | 1 MΩ | |
|---|---|---|---|---|
| | Filters Off | Anti-alias Filter On | Filters Off | Anti-alias Filter On |
| 0.2 V | 60 dB | 60 dB | 56 dB | 60 dB |
| 0.4 V | 62 dB | 62 dB | 61 dB | 62 dB |
| 1 V | 62 dB | 62 dB | 62 dB | 62 dB |
| 2 V | 62 dB | 62 dB | 62 dB | 62 dB |
| 4 V | — | — | 61 dB | 62 dB |

11. 10 MHz, -1 dBFS input signal. Includes the 2nd through the 5th harmonics.
12. 0.2 V to 2.0 V input range. 50 Ω input impedance. Two tones at 10.2 MHz and 11.2 MHz. Each tone is -7 dBFS.
13. 10 MHz, -1 dBFS input signal. Excludes harmonics. Measured from DC to 50 MHz.

Table 9. Signal to Noise and Distortion (SINAD)[14]

| Range ($V_{pk-pk}$) | 50 Ω | | 1 MΩ | |
|---|---|---|---|---|
| | Filters Off | Anti-alias Filter On | Filters Off | Anti-alias Filter On |
| 0.2 V | 60 dB | 60 dB | 56 dB | 59 dB |
| 0.4 V | 62 dB | 62 dB | 60 dB | 61 dB |
| 1 V | 62 dB | 62 dB | 61 dB | 61 dB |
| 2 V | 62 dB | 62 dB | 61 dB | 61 dB |
| 4 V | — | — | 60 dB | 61 dB |

Figure 3. PXI-5122 Dynamic Performance, 50 Ω, 1 V Range, Measured

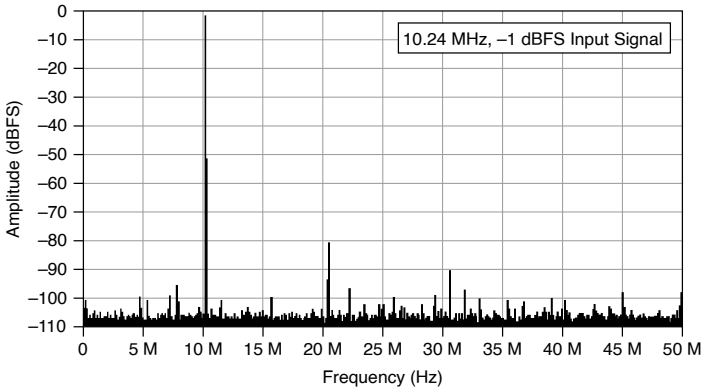



Table 10. RMS Noise (Noise Filter On)[15][15]

| Range ($V_{pk-pk}$) | 50 Ω | 1 MΩ |
|---|---|---|
| 0.2 V | 46 $\mu V_{rms}$ (0.023% FS) | 60 $\mu V_{rms}$ (0.030% FS) |
| 0.4 V | 92 $\mu V_{rms}$ (0.023% FS) | 92 $\mu V_{rms}$ (0.023% FS) |
| 1 V | 230 $\mu V_{rms}$ (0.023% FS) | 230 $\mu V_{rms}$ (0.023% FS) |
| 2 V | 460 $\mu V_{rms}$ (0.023% FS) | 460 $\mu V_{rms}$ (0.023% FS) |
| 4 V | 920 $\mu V_{rms}$ (0.023% FS) | 920 $\mu V_{rms}$ (0.023% FS) |
| 10 V | 2.3 $mV_{rms}$ (0.023% FS) | 2.3 $mV_{rms}$ (0.023% FS) |
| 20 V | — | 4.6 $mV_{rms}$ (0.023% FS) |

14. 10 MHz, -1 dBFS input signal. Includes harmonics. Measured from DC to 50 MHz.
15. 50 Ω terminator connected to input.

Table 11. RMS Noise (Anti-alias Filter On)[15]

| Range ($V_{pk-pk}$) | 50 Ω | 1 MΩ |
|---|---|---|
| 0.2 V | 66 $\mu V_{rms}$ (0.033% FS) | 80 $\mu V_{rms}$ (0.040% FS) |
| 0.4 V | 100 $\mu V_{rms}$ (0.025% FS) | 120 $\mu V_{rms}$ (0.030% FS) |
| 1 V | 250 $\mu V_{rms}$ (0.025% FS) | 300 $\mu V_{rms}$ (0.030% FS) |
| 2 V | 500 $\mu V_{rms}$ (0.025% FS) | 600 $\mu V_{rms}$ (0.030% FS) |
| 4 V | 1 $mV_{rms}$ (0.025% FS) | 1.2 $mV_{rms}$ (0.030% FS) |
| 10 V | 2.5 $mV_{rms}$ (0.025% FS) | 3 $mV_{rms}$ (0.030% FS) |
| 20 V | — | 6 $mV_{rms}$ (0.030% FS) |

Table 12. RMS Noise (Filters Off)[15]

| Range ($V_{pk-pk}$) | 50 Ω | 1 MΩ |
|---|---|---|
| 0.2 V | 66 $\mu V_{rms}$ (0.033% FS) | 110 $\mu V_{rms}$ (0.055% FS) |
| 0.4 V | 100 $\mu V_{rms}$ (0.025% FS) | 160 $\mu V_{rms}$ (0.040% FS) |
| 1 V | 250 $\mu V_{rms}$ (0.025% FS) | 300 $\mu V_{rms}$ (0.030% FS) |
| 2 V | 500 $\mu V_{rms}$ (0.025% FS) | 600 $\mu V_{rms}$ (0.030% FS) |
| 4 V | 1 $mV_{rms}$ (0.025% FS) | 1.6 $mV_{rms}$ (0.040% FS) |
| 10 V | 2.5 $mV_{rms}$ (0.025% FS) | 3 $mV_{rms}$ (0.030% FS) |
| 20 V | — | 6 $mV_{rms}$ (0.030% FS) |

Figure 4. PXI-5122 Spectral Noise Density, 0.2 V Input Range, Full Bandwidth, 50 Ω Input Impedance, Nominal

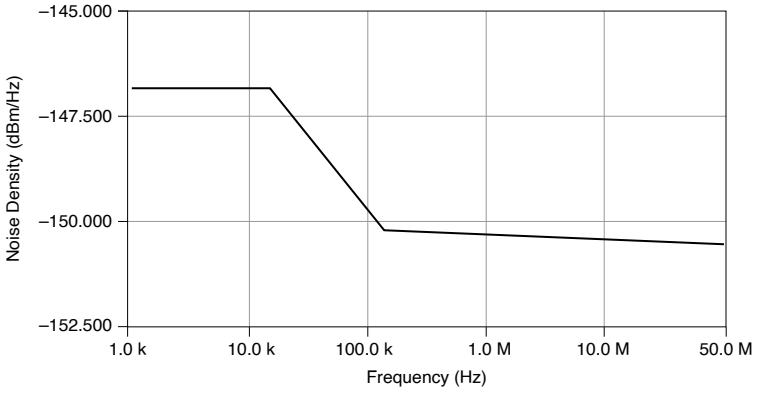
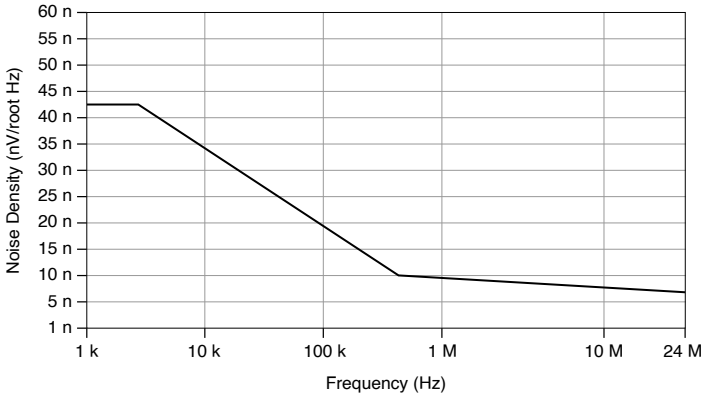


Figure 5. PXI-5122 Spectral Noise Density, 0.2 V Input Range, Noise Filter Enabled, 1 MΩ Input Impedance, Nominal




# Horizontal

## Sample Clock

| Sources | |
|---|---|
| Internal | Onboard clock (internal VCXO)[16] |
| External | CLK IN (front panel SMB connector)<br>PXI Star Trigger (backplane connector) |

### Onboard Clock (Internal VCXO)

| Sample rate range | |
|---|---|
| Real-time sampling (single shot)[17] | 1.526 kS/s to 100 MS/s |
| Random interleaved sampling (RIS) | 200 MS/s to 2 GS/s in multiples of 100 MS/s |
| Phase noise density[18] | <-100 dBc/Hz at 100 Hz |

16. Internal Sample clock is locked to the Reference clock or derived from the onboard VCXO.
17. Divide by n decimation used for all rates less than 100 MS/s.

| | |
|---|---|
| | <-120 dBc/Hz at 1 kHz<br><-130 dBc/Hz at 10 kHz |
| Sample clock jitter[19] | ≤1 $ps_{rms}$ (100 Hz to 100 kHz)<br>≤2 $ps_{rms}$ (100 Hz to 1 MHz) |
| Timebase frequency | 100 MHz |
| **Timebase accuracy** | |
| Not phase-locked to Reference clock | ±25 ppm, Warranted |
| Phase-locked to Reference clock | Equal to the Reference clock accuracy |
| Sample clock delay range | ±1 Sample clock period |
| Sample clock delay/adjustment resolution | ≤10 ps |

### Related information:

- For more information about Sample clock and decimation, refer to the NI High-Speed Digitizers Help.

External Sample Clock

| | |
|---|---|
| Sources | CLK IN (front panel SMB connector) |

18. 10 MHz input signal.
19. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

| | |
|---|---|
| | PXI Star Trigger (backplane connector) |
| Frequency range[20] | 30 MHz to 105 MHz (CLK IN)<br>30 MHz to 80 MHz (PXI Star Trigger) |
| Duty cycle tolerance | 45% to 55% |

### Sample Clock Exporting

Table 13. Exported Sample Clock Destinations

| Destination | Maximum Frequency |
|---|---|
| CLK OUT (front panel SMB connector) | 105 MHz |
| PXI_Trig <0..6> (backplane connector)[21][21] | 20 MHz |
| PFI <0..1> (front panel 9-pinmini-circular DIN connector)[21] | 25 MHz |
| RTSI <0..6> [21] | 20 MHz |

## Phase-Locked Loop (PLL) Reference Clock

| | |
|---|---|
| Sources | PXI_CLK10 (backplane connector)<br>CLK IN (front panel SMB connector) |
| Frequency range[22] | 5 MHz to 20 MHz in 1 MHz increments |

20. Divide by n decimation available, where 1 ≤ n ≤ 65,535.
21. Decimated Sample clock only.
22. Default of 10 MHz. The PLL Reference clock frequency must be accurate to ±50 ppm.

| | |
|---|---|
| Duty cycle tolerance | 45% to 55% |
| Exported reference clock destinations | CLK OUT (front panel SMB connector)<br>PFI <0..1> (front panel 9-pinmini-circular DIN connector)<br>PXI_Trig <0..7> |

## CLK IN (Sample Clock and Reference Clock Input)

| | |
|---|---|
| Connector | SMB jack |
| **Input voltage range** | |
| Sine wave ($V_{pk-pk}$) | 0.65 V to 2.8 V (0 dBm to 13 dBm) |
| Square wave ($V_{pk-pk}$) | 0.2 V to 2.8 V |
| Maximum input overload | 7 $V_{rms}$ with \|Peaks\| ≤10 V |
| Impedance | 50 Ω |
| Coupling | AC |

## CLK OUT (Sample Clock and Reference Clock Output)

| | |
|---|---|
| Connector | SMB jack |

| | |
|---|---|
| Output impedance | 50 Ω |
| Logic type | 3.3 V CMOS |
| Maximum drive current | ±48 mA |

# Trigger

## Reference (Stop) Trigger

**Note** Refer to the following sections and the ***NI High-Speed Digitizers Help*** for more information about what sources are available for each trigger type.

| | |
|---|---|
| Trigger types | Edge<br>Window<br>Hysteresis<br>Video<br>Digital<br>Immediate<br>Software |
| Trigger sources | CH 0<br>CH 1<br>TRIG |

| | |
|---|---|
| | PXI_Trig <0..6><br>PFI <0..1><br>PXI Star Trigger<br>Software |
| **Time resolution** | |
| **Time-to-digital conversion circuit (TDC) on** | |
| Onboard clock | 100 ps |
| External clock | N/A |
| **TDC off** | |
| Onboard clock | 10 ns |
| External clock | External clock period |
| **Minimum rearm time**[23] | |
| TDC on | 12 µs |
| TDC off | 3 µs |
| **Holdoff**[24] | |
| Onboard clock | Rearm time to 171.79 s |

23. Holdoff set to 0. Onboard Sample clock at maximum rate.
24. TDC is off when using external Sample clock.

| | |
|---|---|
| External clock | (***Rearm time***/10 ns) × ***External clock period*** to ($2^{34}$ - 1) × ***External clock period*** |

### Analog Trigger

| | |
|---|---|
| Trigger types | Edge<br>Window<br>Hysteresis |
| Sources | CH 0 (front panel BNC connector)<br>CH 1 (front panel BNC connector)<br>TRIG (front panel BNC connector) |

| **Trigger level range** | |
|---|---|
| CH 0, CH 1 | 100% of FS |
| TRIG (external trigger) | ±5 V |
| Trigger level resolution | 10 bits (1 in 1,024) |

| **Edge trigger sensitivity** | |
|---|---|
| CH 0, CH 1 | 2.5% FS up to 50 MHz, increasing to 5% FS at 100 MHz, Warranted |
| TRIG (external trigger, $V_{pk-pk}$) | 0.25 V up to 100 MHz, increasing to 1 V at 200 MHz, Warranted |
| **Level accuracy** | |

| | |
|---|---|
| CH 0, CH 1 | ±3.5% FS up to 10 MHz |
| TRIG (external trigger) | ±0.35 V (±3.5% of FS) up to 10 MHz |
| Trigger jitter | ≤80 $ps_{rms}$ [25] |
| **Trigger filters** | |
| Low-frequency (LF) reject | 50 kHz |
| High-frequency (HF) reject | 50 kHz |

### Digital Trigger

| | |
|---|---|
| Trigger type | Digital |
| Sources | PXI_Trig <0..6> (backplane connector)<br>PFI <0..1> (front panel SMB connector)<br>PXI Star Trigger (backplane connector) |

### Video Trigger

| | |
|---|---|
| Trigger type | Video |
| Sources | CH 0 (front panel BNC connector) |

25. Within ±5 °C of self-calibration temperature.

| | |
|---|---|
| | CH 1 (front panel BNC connector)<br>TRIG (front panel BNC connector) |
| Video trigger types | Specific line<br>Any line<br>Specific field |
| Standards | Negative sync of NTSC, PAL, or SECAM signal |

## External Trigger

| | |
|---|---|
| Connector | TRIG (front panel BNC connector) |
| Impedance | 1 MΩ in parallel with 22 pF |
| Coupling | AC<br>DC |
| AC-coupling cutoff (-3 dB) | 12 Hz |
| Input voltage range | ±5 V |
| Maximum input overload | \|Peaks\| ≤42 V |

# Programmable Function Interface (PFI 0 and PFI 1)

| | |
|---|---|
| Connector | AUX I/O (9-pin mini-circular DIN) |
| Direction | Bi-directional |
| **As an input (trigger)** | |
| Destinations | Start trigger (acquisition arm)<br>Reference (stop) trigger<br>Arm reference trigger<br>Advance trigger |
| Input impedance | 150 kΩ, nominal |
| $V_{IH}$ | 2.0 V |
| $V_{IL}$ | 0.8 V |
| Maximum input overload | -0.5 V to 5.5 V |
| Maximum frequency | 25 MHz |
| **As an output (event)** | |
| Sources | Ready for Start<br>Start trigger (acquisition arm) |

| | |
|---|---|
| | Ready for Reference<br>Reference (stop) trigger<br>End of Record<br>Ready for Advance<br>Advance trigger<br>Done (end of acquisition)<br>Probe Compensation[26] |
| Output impedance | 50 Ω |
| Logic type | 3.3 V CMOS |
| Maximum drive current | ±24 mA |
| Maximum frequency | 25 MHz |

# Waveform

Table 14. Onboard Memory Size

| Memory per Channel | Samples per Channel | Maximum Number of Records in Onboard Memory |
|---|---|---|
| 8 MB (standard option) | 4 MS | 21,845 |
| 32 MB | 16 MS | 87,381 |
| 256 MB | 128 MS | 100,000[27] |

26. 1 kHz, 50% duty cycle square wave, PFI 1 only.
27. It is possible to exceed this number if you fetch records while acquiring data.

| Memory per Channel | Samples per Channel | Maximum Number of Records in Onboard Memory |
|---|---|---|
| 512 MB | 256 MS | 100,000[] |

| | |
|---|---|
| Minimum record length | 1 sample |
| Number of pretrigger samples | Zero up to full record length[28][28] |
| Number of posttrigger samples | Zero up to full record length[28] |
| Allocated onboard memory per record | (Record Length × 2 bytes/S) + 200 bytes, rounded up to next multiple of 128 bytes or 384 bytes, whichever is greater |

**Related information:**

- For more information about fetching records while acquiring data, refer to the NI High-Speed Digitizers Help, available at ni.com/manuals.

# Calibration

## External Calibration

External calibration calibrates the VCXO and the voltage reference. All calibration constants are stored in nonvolatile memory.

## Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.

28. Single-record mode and multiple-record mode.

## Calibration Specifications

| | |
|---|---|
| Interval for external calibration | 2 years |
| Warm-up time[29] | 15 minutes |

# Software

## Driver Software

Driver support for this device was first available in NI-SCOPE2.6.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXI-5122. NI-SCOPE provides application programming interfaces for many development environments.

## Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

## Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXI-5122 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to

29. Warm-up time begins after the NI-SCOPE driver is loaded. Unless manually disabled, the NI-SCOPE driver automatically loads with the operating system and enables the module.

perform interactive measurements on several different device types in a single program.

**Note** InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXI-5122 was first available via InstrumentStudio in NI-SCOPE18.0 and via the NI-SCOPE SFP in NI-SCOPE2.0.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXI-5122. MAX is included on the driver media.

## TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the ***NI-TClk Synchronization Help***, which is located within the ***NI High-Speed Digitizers Help***. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

#### Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Specifications are valid under the following conditions:

- PXI-5122 modules installed in one NI PXI-1042 chassis, or PXIe-5122 modules installed in one PXI Express chassis.
- All parameters set to identical values for each SMC-based module.
- Sample clock set to 100 MS/s and all filters disabled.

**Note** Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

| | |
|---|---|
| Skew[30] | 500 ps |
| Average skew after manual adjustment[31] | <10 ps |
| Sample clock delay/adjustment resolution | ≤10 ps |

## Power

| **Current draw** | |
|---|---|
| +3.3 V DC | 1.4 A, typical |
| +5 V DC | 1.5 A, typical |
| +12 V DC | 110 mA, typical |
| -12 V DC | 270 mA, typical |
| Total power | 16.7 W, typical |

## Dimensions and Weight

| | |
|---|---|
| Dimensions | 3U, one-slot, PXI/cPCI module |

30. Caused by clock and analog path delay differences. No manual adjustment performed.
31. For information about manual adjustment, refer to the ***Synchronization Repeatability Optimization*** topic in the ***NI-TClk Synchronization Help*** available at ni.com/manuals. For additional help with the adjustment process, contact NI Technical Support at ni.com/support.

| | |
|---|---|
| | 21.6 cm × 2.0 cm × 13.0 cm<br>(8.5 in. × 0.8 in. × 5.1 in.) |
| Weight | 383 g (13.5 oz) |

# Environment

| | |
|---|---|
| Maximum altitude | 2,000 m (at 25 °C ambient temperature) |
| Pollution Degree | 2 |

Indoor use only.

## Operating Environment

| | |
|---|---|
| Ambient temperature range | 0 °C to 45 °C when installed in an NI PXI-1000/B or PXI-101x chassis.<br>0 °C to 55 °C when installed in any other NI PXI chassis.<br>(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) |
| Relative humidity range | 10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.) |

## Storage Environment

| | |
|---|---|
| Ambient temperature range | -40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) |

| | |
|---|---|
| Relative humidity range | 5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.) |

# Shock and Vibration

| | |
|---|---|
| Operational shock | 30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.) |
| Storage shock | 50 g peak, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.) |
| **Random vibration** | |
| Operating | 5 Hz to 500 Hz, 0.31 $g_{rms}$ (Tested in accordance with IEC 60068-2-64.) |
| Nonoperating | 5 Hz to 500 Hz, 2.46 $g_{rms}$ (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.) |

# Compliance and Certifications

## Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

**Note** For safety certifications, refer to the product label or the Product Certifications and Declarations section.

## Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

**Note** In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

**Note** Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

**Note** For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

## Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

## Environmental Management

NI is committed to designing and manufacturing products in an environmentally

responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)