PCIe-6593 Specifications

2025-03-14

Contents

PCIe-6593 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Typical*** unless otherwise noted.

Conditions

Specifications are valid at 25 °C unless otherwise noted.

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[1]

Voltage Family (V)	V_{IL} (V)	V_{IH} (V)	V_{OL} (100 µA Load) (V)	V_{OH} (100 µA Load) (V)	Maximum DC Drive Strength (mA)
3.3	0.8	2.0	0.2	3.0	24
2.5	0.7	1.6	0.2	2.2	18
1.8	0.62	1.29	0.2	1.5	16
1.5	0.51	1.07	0.2	1.2	12
1.2	0.42	0.87	0.2	0.9	6

Digital I/O High-Speed Serial MGT[2]

Data rate	500 Mb/s to 16.375 Gb/s, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O coupling	
MGT TX± channels	AC-coupled, includes 100 nF capacitor
MGT RX± channels	DC-coupled, requires external capacitor

Reconfigurable FPGA

The FPGA specifications for the PCIe-6593 vary according to the FPGA option you select at purchase.

Table 3. Specifications for PCIe-6593 Reconfigurable FPGA Options

	KU040	KU060
LUTs	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,920	2,760
Embedded Block RAM	21.1 Mb	38.0 Mb
Default timebase	80 MHz	
Timebase reference sources	Onboard 100 MHz oscillator	
Data transfers	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA channels	60	

Note The table above depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O.

Note For FPGA designs using the majority of KU040 or KU060 FPGA resources while running at clock rates over 150 MHz, the module may require more power than is available. If the module attempts to draw more than allowed per its specification, the module protects itself and reverts to a default FPGA personality.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit

LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

PORT 0, PORT 1

Data rate	500 Mb/s to 16.3 Gb/s
Connector	QSFP, SFF-8436 compliant
Number of channels	8 RX/TX (GTH)
Supported high-speed cable type	Electrical/optical
Optical cable power	3.3 V ±5%, 1 A per port

MGT TX± Channels[3]

Minimum differential output voltage[4]	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
> 6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal
Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor

MGT Reference Clock Generator

Supported generated frequencies	60.000 MHz to 385.714 MHz 400.000 MHZ to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHz to 771.428 MHz 800 MHz
Clocking resources	PXIe_CLK100 REF/CLK IN
Available MGT Reference Clocks	3

CLK OUT

Connector type	SMA
Coupling	AC
Output impedance	50 Ω, nominal
Supported output frequencies	2.344 MHz to 385.714 MHz 400.000 MHz to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHz to 771.428 MHz 800.000 MHz to 900.000 MHz 960.000 MHz to 1000.000 MHz
Output voltage range	0.61 V pk-pk to 1.04 V pk-pk

REF/CLK IN

Connector type	SMA
Input coupling	AC
Input impedance	50 Ω

Frequency range	10 MHz to 300 MHz
Input voltage range	0.3 V pk-pk to 4 V pk-pk
Absolute maximum voltage	5 V pk-pk AC
Duty cycle	45% to 55%

Bus Interface

Card edge form factor	PCI Express Gen-3 x8
Slot compatibility	x8 and x16 PCI Express

Maximum Power Requirements

Note Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V, supplied by card edge connector	4.5 A
+12 V, supplied by 6-pin PCI Express power connector	5 A
Maximum total power	60 W

Physical

Dimensions (including I/O bracket, not including connectors)	12.6 cm × 26.3 cm × 4 cm (5.0 in. × 10.4 in. × 1.6 in.)
Weight	990 g (35 oz)
PCI Express mechanical form factor	Standard height, three-quarter length, double slot
Integrated air mover (fan)	Yes
Maximum rear panel exhaust airflow	84 m^3/h (50 CFM) (without any chassis impedance)

Environmental Characteristics

Temperature	
Operating , local[5]	0 °C to 45 °C
Storage	-20 °C to 70 °C
Humidity	
Operating	10% to 90% RH, noncondensing
Storage	5% to 95% RH, noncondensing

Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)