NI-6585/6585B Getting Started

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Contents

NI 6585/6585B Getting Started

Note Before you begin, complete the software and hardware installation instructions in your FlexRIO FPGA getting started guide or controller for FlexRIO getting started guide.

Caution Using the NI 6585/6585B in a manner not described in this document may impair the protection the NI 6585/6585B provides.

The NI 6585/6585B is a low-voltage differential (LVDS) adapter module designed to work in conjunction with FlexRIO FPGA modules and controllers for FlexRIO.

This document explains how to install and configure the NI 6585/6585B.

Note ***NI 6585R*** refers to the combination of your NI 6585/6585B adapter module and either a FlexRIO FPGA module or a controller for FlexRIO. NI 6585/6585B refers to your adapter module only.

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by NI could

void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots. You can order a kit of six single slot EMC Filler Panels directly from NI by visiting ni.com.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 30 m (100 ft).

Caution Using the NI 6585/6585B in a manner not described in this document may impair the protection the NI 6585/6585B provides.

FlexRIO Documentation

Table 1. FlexRIO Documentation Locations and Descriptions

Document	Location	Description
Getting started guide for your FlexRIO FPGA module or controller for FlexRIO	Available from the Start menu and at ni.com/manuals.	Contains installation instructions for your FlexRIO system.
Specifications document for your FlexRIO FPGA module or controller for FlexRIO	Available from the Start menu and at ni.com/manuals.	Contains specifications for your FlexRIO FPGA module or controller for FlexRIO.
Getting started guide for your adapter module	Available from the Start menu and at ni.com/manuals.	Contains signal information, examples, and CLIP details for your adapter module.
Specifications document for your adapter module	Available from the Start menu and at ni.com/manuals.	Contains specifications for your adapter module.
LabVIEW FPGA Module Help	Embedded in ***LabVIEW Help*** and at ni.com/manuals.	Contains information about the basic functionality of the LabVIEW FPGA Module.

Document	Location	Description
Real-Time Module Help	Embedded in ***LabVIEW Help*** and at ni.com/manuals.	Contains information about real-time programming concepts, step-by-step instructions for using LabVIEW with the Real-Time Module, reference information about Real-Time Module VIs and functions, and information about LabVIEW features on real-time operating systems.
FlexRIO Help	Available from the Start menu and at ni.com/manuals.	Contains information about the FPGA module front panel connectors and I/O, controller for FlexRIO front panel connectors and I/O, programming instructions, and adapter module component-level IP (CLIP).
LabVIEW Examples	Available in NI Example Finder. In LabVIEW, click **Help** » **Find Examples** » **Hardware Input and Output** » **FlexRIO**.	Contains examples of how to run FPGA VIs and Host VIs on your device.
IPNet	Located at ni.com/ipnet.	Contains LabVIEW FPGA functions and intellectual property to share.
FlexRIO product page	Located at ni.com/flexrio.	Contains product information and data sheets for FlexRIO devices.

FlexRIO Examples

FlexRIO includes several example applications for LabVIEW. These examples serve as interactive tools, programming models, and as building blocks in your own applications.

Accessing FlexRIO Examples

FlexRIO examples are available in LabVIEW's NI Example Finder. Complete the following steps to access the examples by task.

1. In LabVIEW, click **Help** » **Find Examples**.
2. In the NI Example Finder window that appears, click **Hardware Input and Output** » **FlexRIO**.

   Click on an example and refer to the Information window for a description of the example. Refer the Requirements window for a list of hardware that can run the example.

   You can also click the Search tab to search all installed examples by keyword. For example, search for `FlexRIO` to locate all FlexRIO examples.

Online examples are also available to demonstrate FlexRIO basics, such as using DRAM, acquiring data from adapter modules, and performing high throughput streaming. To access these examples, search `FlexRIO examples` in the **Search the community** field at ni.com/examples.

Verifying the System Requirements

To use the NI 6585/6585B, your system must meet certain requirements. For more information about minimum system requirements, recommended system, and supported application development environments (ADEs), refer to the readme, which is installed or available at ni.com/manuals.

Compatibility with FPGA Modules and Controllers for FlexRIO

The NI 6585B variant is compatible with all FlexRIO FPGA modules and Controllers for FlexRIO; however, the NI 6585 variant is only compatible with NI PXI-795xR and NI PXIe-796xR modules. The following table lists each adapter module's compatibility with FlexRIO FPGA modules and Controllers for FlexRIO.

Table 2. Adapter Module Compatibility

	NI PXI-795xR	NI PXIe-796xR	NI PXIe-797xR	NI-793xR
NI 6585	Yes	Yes	No	No
NI 6585B	Yes	Yes	Yes	Yes

Unpacking

Caution To prevent ESD from damaging the devices, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.

1. Touch the antistatic package to a metal part of the computer chassis.
2. Remove each module from the package and inspect it for loose components or any other sign of damage.

   Notice Never touch the exposed pins of connectors.

   Note Do not install a device if it appears damaged in any way.

3. Unpack any other items and documentation from the kit.

Store the devices in the antistatic package when they are not in use.

Preparing the Environment

Ensure that the environment where you are using the NI 6585/6585B meets the following specifications.

Operating temperature (IEC 60068-2-1, IEC 60068-2-2)	0 °C to 55 °C
Operating humidity (IEC 60068-2-56)	10% to 90% RH, noncondensing

Pollution Degree	2
Maximum altitude	2,000 m at 25 °C ambient temperature

Indoor use only.

Note Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.

Installing the NI 6585/6585B

Refer to the getting started guide for your FlexRIO FPGA module or Controller for FlexRIO for instructions about how to install your FlexRIO system, including the NI 6585/6585B.

Confirming that Measurement & Automation Explorer (MAX) Recognizes the Device

Use Measurement & Automation Explorer (MAX) to configure your NI hardware. MAX informs other programs about which devices reside in the system and how they are configured. MAX is automatically installed with FlexRIO Support.

1. Launch MAX by navigating to **Start** » **All Programs** » **National Instruments** » **NI MAX** or by clicking the NI MAX desktop icon.
2. In the Configuration pane, double-click **Devices and Interfaces** to see the list of installed devices. Installed devices appear under the name of their associated chassis.
3. (PXI and PXI Express devices only) Expand your **Chassis** tree item. MAX lists all devices installed in the chassis. Your default device names may vary.

   Note If you do not see your hardware listed, press <F5> to refresh the list

of installed devices. If the device is still not listed, power off the system, ensure the device is correctly installed, and restart.

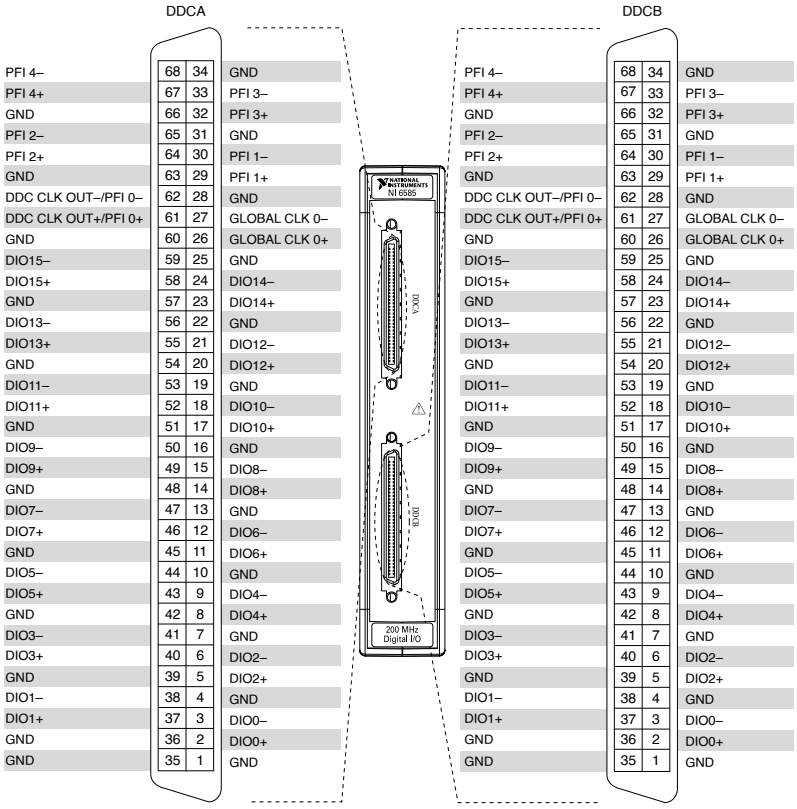
4. (Controllers for FlexRIO only) Your device appears under the **Remote Devices** section.

Front Panel and Connector Pinouts

The following figure shows the front panel connectors for the NI 6585/6585B.

Note For more information about the NI 6585/6585B front panel connectors, refer to the NI 6585/6585B Specifications.

Figure 1. NI 6585/6585B Connector Pin Assignments



DDCA				DDCB			
PFI 4–	68	34	GND	PFI 4–	68	34	GND
PFI 4+	67	33	PFI 3–	PFI 4+	67	33	PFI 3–
GND	66	32	PFI 3+	GND	66	32	PFI 3+
PFI 2–	65	31	GND	PFI 2–	65	31	GND
PFI 2+	64	30	PFI 1–	PFI 2+	64	30	PFI 1–
GND	63	29	PFI 1+	GND	63	29	PFI 1+
DDC CLK OUT–/PFI 0–	62	28	GND	DDC CLK OUT–/PFI 0–	62	28	GND
DDC CLK OUT+/PFI 0+	61	27	GLOBAL CLK 0–	DDC CLK OUT+/PFI 0+	61	27	GLOBAL CLK 0–
GND	60	26	GLOBAL CLK 0+	GND	60	26	GLOBAL CLK 0+
DIO15–	59	25	GND	DIO15–	59	25	GND
DIO15+	58	24	DIO14–	DIO15+	58	24	DIO14–
GND	57	23	DIO14+	GND	57	23	DIO14+
DIO13–	56	22	GND	DIO13–	56	22	GND
DIO13+	55	21	DIO12–	DIO13+	55	21	DIO12–
GND	54	20	DIO12+	GND	54	20	DIO12+
DIO11–	53	19	GND	DIO11–	53	19	GND
DIO11+	52	18	DIO10–	DIO11+	52	18	DIO10–
GND	51	17	DIO10+	GND	51	17	DIO10+
DIO9–	50	16	GND	DIO9–	50	16	GND
DIO9+	49	15	DIO8–	DIO9+	49	15	DIO8–
GND	48	14	DIO8+	GND	48	14	DIO8+
DIO7–	47	13	GND	DIO7–	47	13	GND
DIO7+	46	12	DIO6–	DIO7+	46	12	DIO6–
GND	45	11	DIO6+	GND	45	11	DIO6+
DIO5–	44	10	GND	DIO5–	44	10	GND
DIO5+	43	9	DIO4–	DIO5+	43	9	DIO4–
GND	42	8	DIO4+	GND	42	8	DIO4+
DIO3–	41	7	GND	DIO3–	41	7	GND
DIO3+	40	6	DIO2–	DIO3+	40	6	DIO2–
GND	39	5	DIO2+	GND	39	5	DIO2+
DIO1–	38	4	GND	DIO1–	38	4	GND
DIO1+	37	3	DIO0–	DIO1+	37	3	DIO0–
GND	36	2	DIO0+	GND	36	2	DIO0+
GND	35	1	GND	GND	35	1	GND

Caution To avoid permanent damage to the NI 6585/6585B, disconnect all signals connected to the NI 6585/6585B before powering down the module, and connect signals only after the adapter module has been powered on by the FlexRIO FPGA module or Controller for FlexRIO.

Caution Connections that exceed any of the maximum ratings of any connector on the NI 6585/6585B can damage the device and the chassis. NI is not liable for any damage resulting from such connections.

Related information:

- NI 6585/6585B Specifications

Pinout and Signal Information

The following table contains pin location and signal information for the NI 6585/6585B.

Note DIO <0..15>+/-, PFI <0..4>+/-, and DDC CLOCK OUT appear on both connectors, DDCA and DDCB.

Note PFI <0> can be used as an IO port. You can modify the CLIP for the NI 6585B to expose the signal as PFI <0>.

Table 3. DDC Connector Pins

Signal Name	Pin(s)	Signal Type	Signal Description
GLOBAL CLOCK 0+	26 on DDCA	Clock	Input terminal for the external clock source, which can be used for dynamic acquisition or generation.
GLOBAL CLOCK 0-	27 on DDCA		
GLOBAL CLOCK 1+	26 on DDCB		
GLOBAL CLOCK 1-	27 on DDCB		
DIO <0..15>+	2, 5, 8 ,11 ,14, 17, 20, 23, 37, 40, 43, 46, 49, 52, 55 , 58	Data	Positive terminal of LVDS digital I/O data channels 0 through 15.
DIO <0..15>-	3, 6, 9, 12, 15, 18, 21, 24, 38, 41, 44, 47, 50, 53, 56, 59	Data	Negative terminal of LVDS digital I/O data channels 0 through 15.
DDC CLOCK OUT+/PFI 0+	61	Clock/Data	Positive output terminal for the exported Sample clock/Positive

Signal Name	Pin(s)	Signal Type	Signal Description
			Programmable Function Interface terminal 0
DDC CLOCK OUT-/PFI 0-	62	Clock/Data	Negative output terminal for the exported Sample clock/Negative Programmable Function Interface terminal 0
PFI <1..4>+	29, 64, 32, 67	Data	Positive terminal of the Programmable Function Interface LVDS digital I/O channels 1 through 4.
PFI <1..4>-	30, 65, 33, 68	Data	Negative terminal of the Programmable Function Interface LVDS digital I/O channels 1 through 4.
GND	1, 4, 7, 10, 13, 16, 19, 22, 25, 28, 31, 34, 35, 36, 39, 42, 45, 48, 51, 54, 57, 60, 63, 66	Ground	Ground reference for signals.

The following table lists the NI 6585/6585B connector signals and corresponding FlexRIO FPGA module signals necessary for designing a custom CLIP.

Table 4. NI 6585/6585B Connector Signals and FlexRIO FPGA Module Signals

NI 6585/6585B		FlexRIO FPGA Module		
Connector	**Signal Name**	**GPIO Out**	**GPIO Out Enable**	**GPIO In**
DDCA	GLOBAL CLOCK 0	—	—	GClk_SE
	DIO 0+/-	GPIO_30_n	GPIO_31	GPIO_31_n
	DIO 1+/-	GPIO_12_n	GPIO_13	GPIO_13_n
	DIO 2+/-	GPIO_32	GPIO_32_n	GPIO_15_n

NI 6585/6585B		FlexRIO FPGA Module		
Connector	**Signal Name**	**GPIO Out**	**GPIO Out Enable**	**GPIO In**
	DIO 3+/-	GPIO_14	GPIO_14_n	GPIO_15
	DIO 4+/-	GPIO_27_n	GPIO_28	GPIO_28_n
	DIO 5+/-	GPIO_9_n	GPIO_10	GPIO_10_n
	DIO 6+/-	GPIO_29	GPIO_29_n	GPIO_30
	DIO 7+/-	GPIO_11	GPIO_11_n	GPIO_12
	DIO 8+/-	GPIO_22	GPIO_22_n	GPIO_23
	DIO 9+/-	GPIO_6_n	GPIO_7	GPIO_7_n
	DIO 10+/-	GPIO_26	GPIO_26_n	GPIO_27
	DIO 11+/-	GPIO_8	GPIO_8_n	GPIO_9
	DIO 12+/-	GPIO_19	GPIO_19_n	GPIO_20
	DIO 13+/-	GPIO_3_n	GPIO_4	GPIO_4_n
	DIO 14+/-	GPIO_20_n	GPIO_21	GPIO_21_n
	DIO 15+/-	GPIO_5	GPIO_5_n	GPIO_6
	DDC CLOCK OUT+/PFI 0+ DDC CLOCK OUT-/PFI 0-	GPIO_0	GPIO_0_n	GPIO_23_n
	PFI 1+/-	GPIO_1	GPIO_1_n	GPIO_24
	PFI 2+/-	GPIO_16	GPIO_16_n	GPIO_24_n
	PFI 3+/-	GPIO_17	GPIO_17_n	GPIO_25
	PFI 4+/-	GPIO_18	GPIO_18_n	GPIO_25_n

Table 5. NI 6585/6585B Connector Signals and FlexRIO FPGA Module Signals (Continued)

NI 6585/6585B		FlexRIO FPGA Module		
Connector	**Signal Name**	**GPIO Out**	**GPIO Out Enable**	**GPIO In**
DDCB	GLOBAL CLOCK 1	—	—	GClk_LVDS
	DIO 0+/-	GPIO_46	GPIO_46_n	GPIO_47
	DIO 1+/-	GPIO_62_n	GPIO_63	GPIO_63_n

NI 6585/6585B		FlexRIO FPGA Module		
Connector	Signal Name	GPIO Out	GPIO Out Enable	GPIO In
	DIO 2+/-	GPIO_47_n	GPIO_48	GPIO_48_n
	DIO 3+/-	GPIO_64	GPIO_64_n	GPIO_65
	DIO 4+/-	GPIO_43	GPIO_43_n	GPIO_44
	DIO 5+/-	GPIO_59_n	GPIO_60	GPIO_60_n
	DIO 6+/-	GPIO_44_n	GPIO_45	GPIO_45_n
	DIO 7+/-	GPIO_61	GPIO_61_n	GPIO_62
	DIO 8+/-	GPIO_39	GPIO_39_n	GPIO_40
	DIO 9+/-	GPIO_54	GPIO_54_n	GPIO_55
	DIO 10+/-	GPIO_40_n	GPIO_41	GPIO_41_n
	DIO 11+/-	GPIO_55_n	GPIO_56	GPIO_56_n
	DIO 12+/-	GPIO_36	GPIO_36_n	GPIO_37
	DIO 13+/-	GPIO_51	GPIO_51_n	GPIO_52
	DIO 14+/-	GPIO_37_n	GPIO_38	GPIO_38_n
	DIO 15+/-	GPIO_52_n	GPIO_53	GPIO_53_n
	DDC CLOCK OUT+/PFI 0+ DDC CLOCK OUT-/PFI 0-	GPIO_49	GPIO_49_n	GPIO_57
	PFI 1+/-	GPIO_50	GPIO_50_n	GPIO_57_n
	PFI 2+/-	GPIO_33	GPIO_33_n	GPIO_58
	PFI 3+/-	GPIO_34	GPIO_34_n	GPIO_58_n
	PFI 4+/-	GPIO_35	GPIO_35_n	GPIO_59

Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. FlexRIO devices support two types of CLIP: user-defined and socketed.

- ***User-defined CLIP*** allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- ***Socketed CLIP*** provides the same IP integration of the user-defined CLIP, but it also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The NI 6585/6585B ships with socketed CLIP items that add module I/O to the LabVIEW project.

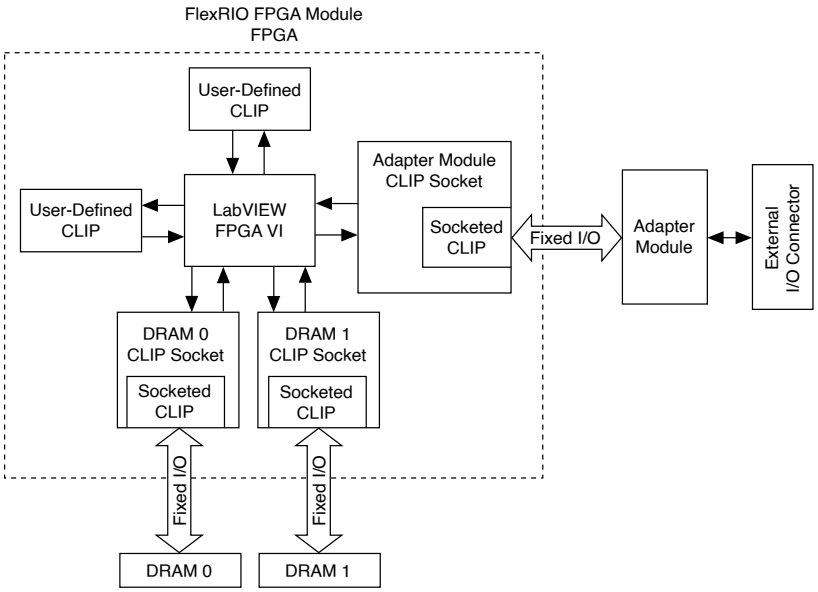
Refer to ***Configuring Your Adapter Module Using LabVIEW FPGA*** in FlexRIO documentation for more information about CLIP.

CLIP and LabVIEW FPGA

The interface between the NI 6585/6585B CLIP and LabVIEW FPGA in the following figures.

If you are using a FlexRIO FPGA module with a Virtex-5 FPGA, refer to the following figure, which shows the relationship between the CLIP and an FPGA VI configured for use with a Virtex-5 FPGA target.

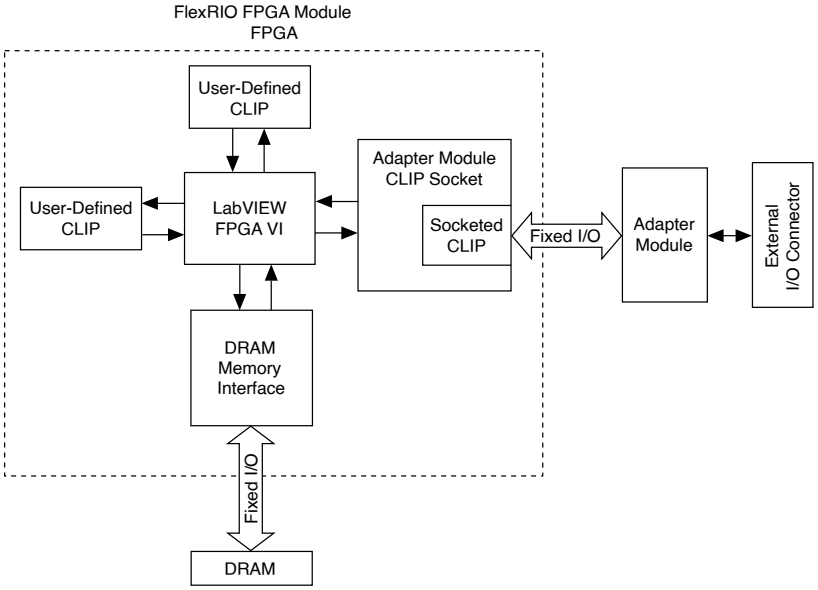
Figure 1. CLIP and FPGA VI Relationship (Virtex-5)



If you are using a FlexRIO FPGA module or Controller for FlexRIO with a Kintex-7 FPGA,

refer to the following figure, which shows the relationship between the CLIP and an FPGA VI configured for use with a Kintex-7 FPGA target.

Figure 1. CLIP and FPGA VI Relationship (Kintex-7)



NI 6585/6585B CLIP

The NI 6585/6585B ships with socketed CLIP that adds module I/O to the LabVIEW project. The NI-developed NI 6585/6585B CLIP are as follows:

- **NI 6585 Basic Channel**—Provides read/write access to all low-voltage differential signal (LVDS) channels using a simple channel-based interface. Each I/O line has a write enable signal. This CLIP provides a clock signal for export on each connector. The clock inputs from the NI 6585 are passed to LabVIEW FPGA for use in the FPGA VI. This CLIP also allows for individual clock output inversion.
- **NI 6585 Basic Connector CLIP**—Provides read/write access to all low-voltage differential signal (LVDS) lines on each connector, where the lines are grouped per connector. The individual data lines for each connector are accessed using a U16 data type in LabVIEW FPGA. Each I/O line has a write enable signal. This CLIP also allows for individual clock output inversion.
- **NI 6585 DDR Connector CLIP**—Provides read/write access to all low-voltage differential signal (LVDS) lines on each connector, where the lines are grouped per connector. The individual datalines for each connector are accessed using a U16 data type in LabVIEW FPGA. Data from each edge of the clock is presented as “rising” and “falling.” Each I/O line has a write enable signal. This CLIP also allows for individual clock output inversion.

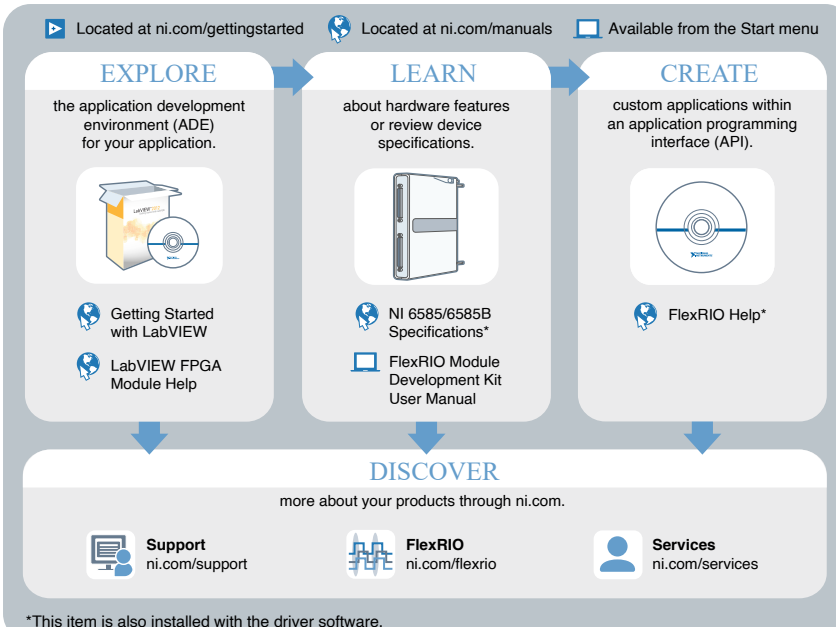
Note Refer to the FlexRIO Help for information about FlexRIO CLIP, configuring the NI 6585/6585B with a socketed CLIP, and a list of available socketed CLIP and provided signals.

Related information:

- FlexRIO User Manual

Where to Go Next

Refer to the following figure for information about other product tasks and associated resources for those tasks.



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