SLSC-12101 Specifications

2025-03-10

Contents

SLSC-12101 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Typical-95*** specifications describe the performance met by 95% (≈2σ) of models with a 95% confidence.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Warranted*** unless otherwise noted.

Specifications are ***Characteristic*** unless otherwise noted.

Specifications are ***Typical*** unless otherwise noted.

Specifications are ***Nominal*** unless otherwise noted.

Specifications are ***Measured*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- The SLSC-12101 module is mounted in an SLSC chassis with the recommended cooling clearances and using a power supply that meets the specifications provided in the chassis user guide.
- For the entire temperature range of the chassis.

Note These specifications only apply to the product as provided by NI. Modifications to the module may invalidate these. Be certain to verify the performance of modified modules.

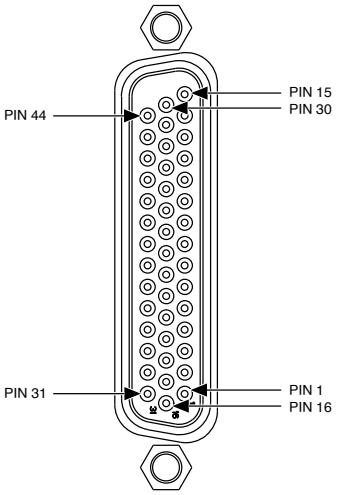
Caution Observe all instructions and cautions in the user documentation. Using the model in a manner not specified can damage the model and compromise the built-in safety protection. Return damaged models to NI for repair.

SLSC-12101 Pinout

Front I/O Connector Pinout

See the following image for the front I/O connector pinout.

Figure 1. Front Connector Pinout



Prototyping Area

The front connectors J10 and J11 (labeled J1 and J2 on the front panel) are routed directly to the prototyping area without any series resistors. The traces have 50 Ω characteristic impedance and support a maximum of 400 mA.

All signals from the CPLD to the prototyping area are routed with 50 Ω characteristic impedance traces and have a 33.2 Ω series resistor places near the CPLD.

All connections between XJ2 and the RTI prototyping area are routed with 50 Ω characteristic impedance without any series resistors.

The connections between XJ3 and the RTI prototyping area with high current traces are capable of carrying 8 A each. For more information, refer to the SLSC-12101 Specifications, which can be found on ni.com/manuals.

Hole Marking Codes

Table 1. Marking Codes to Identify the Holes in the Prototyping Area

Unconnected	Ground	Signal	Power
			
Unconnected holes do not have any silkscreen marking. These holes can be used for any connections. An example of this kind of hole is M8 of Bank 1.	Holes connected to ground are marked with a solid white square (represented in black in this document). An example of this type of hole is AD4 of Bank 2.	Holes connected to a trace have a box around them. The box can be a rectangle around adjacent holes connected to traces. An example of this type of hole is C18 of Bank 3. An example of a rectangle enclosing adjacent holes are holes AB7 to AB9 of Bank 3. The rectangles have labels attached providing an indication	Holes connected to power rails have a circle around them. An example of this hole is A23 of Bank 4, which is a hole connected to the 5 V rail. These may also have boxes around them to help with labeling.

Unconnected	Ground	Signal	Power
		of which signals these are. For example, C18 of Bank 3 is labeled CPLD(133) and holes AB7 to AB9 are labeled CPLD(134:136).	

Bank 1 Prototyping Area

Figure 1. Bank 1 Prototyping Area

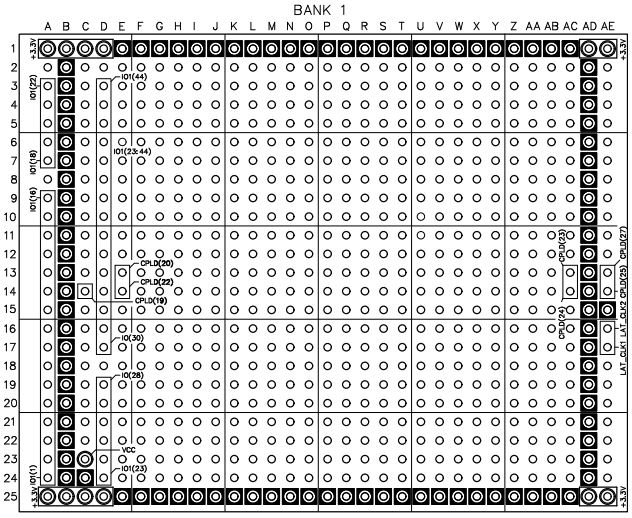


Table 2. CPLD Connectivity to Bank 1 Prototyping Area

Bank 1 Lattice					
Lattice Location	**Schematic Name**[1]	**CPLD Bank**	**CPLD Pin**	**HDL Name**	**Physical Channel Name**
C14	Bank1_IO(19)	1	G3	cBank1ioA(0)	Bank1_PortA_DIO0
E13	Bank1_IO(20)	1	G4	cBank1ioA(1)	Bank1_PortA_DIO1
E14	Bank1_IO(22)	1	H1	cBank1ioA(2)	Bank1_PortA_DIO2
AC13	Bank1_IO(23)	1	H2	cBank1ioA(3)	Bank1_PortA_DIO3
AC14	Bank1_IO(24)	1	H3	cBank1ioA(4)	Bank1_PortA_DIO4
AE14	Bank1_IO(25)	1	H4	cBank1ioA(5)	Bank1_PortA_DIO5
AE13	Bank1_IO(27)	1	J1	cBank1ioA(6)	Bank1_PortA_DIO6

1. In the silkscreen, these signals are marked CPLD(Pin Number) for space reasons.

Table 3. Connector 1 Connectivity to Bank 1 Prototyping Area

Connector J1					
J1 Pin	**Schematic Name**[2]	**Lattice Coordinate (Bank 1)**	**J1 Pin**	**Schematic Name**[3]	**Lattice Coordinate (Bank 1)**
1	Front1_IO(1)	A24	23	Front1_IO(23)	D24
2	Front1_IO(2)	A23	24	Front1_IO(24)	D23
3	Front1_IO(3)	A22	25	Front1_IO(25)	D22
4	Front1_IO(4)	A21	26	Front1_IO(26)	D21
5	Front1_IO(5)	A20	27	Front1_IO(27)	D20
6	Front1_IO(6)	A19	28	Front1_IO(28)	D19
7	Front1_IO(7)	A18	29	GND	GND
8	Front1_IO(8)	A17	30	Front1_IO(30)	D17
9	Front1_IO(9)	A16	31	Front1_IO(31)	D16
10	Front1_IO(10)	A15	32	Front1_IO(32)	D15
11	Front1_IO(11)	A14	33	Front1_IO(33)	D14
12	Front1_IO(12)	A13	34	Front1_IO(34)	D13
13	Front1_IO(13)	A12	35	Front1_IO(35)	D12
14	Front1_IO(14)	A11	36	Front1_IO(36)	D11
15	Front1_IO(15)	A10	37	Front1_IO(37)	D10
16	Front1_IO(16)	A9	38	Front1_IO(38)	D9
17	GND	GND	39	Front1_IO(39)	D8
18	Front1_IO(18)	A7	40	Front1_IO(40)	D7
19	Front1_IO(19)	A6	41	Front1_IO(41)	D6
20	Front1_IO(20)	A5	42	Front1_IO(42)	D5
21	Front1_IO(21)	A4	43	Front1_IO(43)	D4
22	Front1_IO(22)	A3	44	Front1_IO(44)	D3

2. In the silkscreen, these signals are marked IO1(Pin Number) for space reasons.
3. In the silkscreen, these signals are marked IO1(Pin Number) for space reasons.

Table 4. Miscellaneous Signals In Bank 1 Prototyping Area

Miscellaneous Signals			
Coordinate	**Signal**	**Coordinate**	**Signal**
A1-D1	3.3 V	B2-B24	GND
A25-D15	3.3 V	E25-AC25	GND
AD1	3.3 V	AD2-AD24	GND
AE1	3.3 V	C24	GND
AD25	3.3 V	C23	VCC (5 V)
AE25	3.3 V	AE16	LAT_CLK2
E1-AC1	GND	AE17	LAT_CLK1

Bank 2 Prototyping Area

Figure 1. Bank 2 Prototyping Area

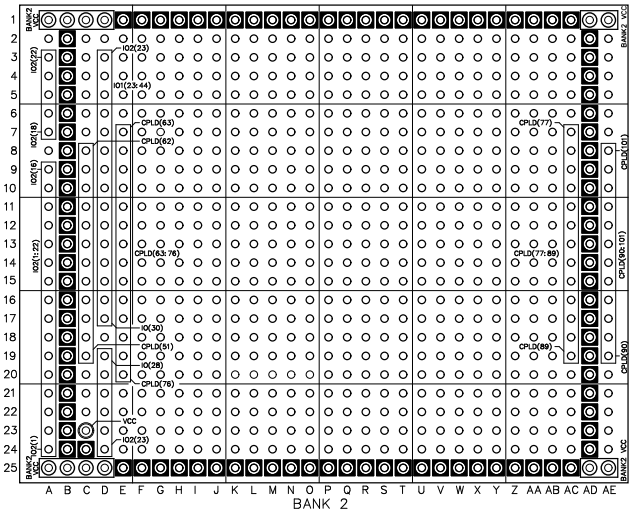


Table 5. CPLD Connectivity to Bank 2 Prototyping Area

Bank 2 Lattice					
Lattice Location	**Schematic Name**	**CPLD Bank**	**CPLD Pin**	**HDL Name**	**Physical Channel Name**
C19	Bank2_IO(51)	2	A10	cBank2ioA(0)	Bank2_PortA_DIO0
C18	Bank2_IO(52)	2	A11	cBank2ioA(1)	Bank2_PortA_DIO1
C17	Bank2_IO(53)	2	A12	cBank2ioA(2)	Bank2_PortA_DIO2

Bank 2 Lattice					
Lattice Location	Schematic Name	CPLD Bank	CPLD Pin	HDL Name	Physical Channel Name
C16	Bank2_IO(54)	2	A13	cBank2ioA(3)	Bank2_PortA_DIO3
C15	Bank2_IO(55)	2	A15	cBank2ioA(4)	Bank2_PortA_DIO4
C14	Bank2_IO(56)	2	A2	cBank2ioA(5)	Bank2_PortA_DIO5
C13	Bank2_IO(57)	2	A4	cBank2ioA(6)	Bank2_PortA_DIO6
C12	Bank2_IO(58)	2	A5	cBank2ioA(7)	Bank2_PortA_DIO7
C11	Bank2_IO(59)	2	A6	cBank2ioB(0)	Bank2_PortB_DIO0
C10	Bank2_IO(60)	2	A7	cBank2ioB(1)	Bank2_PortB_DIO1
C9	Bank2_IO(61)	2	A8	cBank2ioB(2)	Bank2_PortB_DIO2
C8	Bank2_IO(62)	2	A9	cBank2ioB(3)	Bank2_PortB_DIO3
E8	Bank2_IO(64)	2	B10	cBank2ioB(4)	Bank2_PortB_DIO4
E9	Bank2_IO(65)	2	B11	cBank2ioB(5)	Bank2_PortB_DIO5
E10	Bank2_IO(66)	2	B12	cBank2ioB(6)	Bank2_PortB_DIO6
E11	Bank2_IO(67)	2	B13	cBank2ioB(7)	Bank2_PortB_DIO7
E12	Bank2_IO(68)	2	B14	cBank2ioC(0)	Bank2_PortC_DIO0
E13	Bank2_IO(69)	2	B16	cBank2ioC(1)	Bank2_PortC_DIO1
E14	Bank2_IO(70)	2	B3	cBank2ioC(2)	Bank2_PortC_DIO2
E15	Bank2_IO(71)	2	B4	cBank2ioC(3)	Bank2_PortC_DIO3
E16	Bank2_IO(72)	2	B5	cBank2ioC(4)	Bank2_PortC_DIO4
E17	Bank2_IO(73)	2	B6	cBank2ioC(5)	Bank2_PortC_DIO5
E18	Bank2_IO(74)	2	B7	cBank2ioC(6)	Bank2_PortC_DIO6
E19	Bank2_IO(75)	2	B8	cBank2ioC(7)	Bank2_PortC_DIO7
AC8	Bank2_IO(78)	2	C11	cBank2ioD(0)	Bank2_PortD_DIO0
AC9	Bank2_IO(79)	2	C12	cBank2ioD(1)	Bank2_PortD_DIO1
AC10	Bank2_IO(80)	2	C13	cBank2ioD(2)	Bank2_PortD_DIO2
AC11	Bank2_IO(81)	2	C4	cBank2ioD(3)	Bank2_PortD_DIO3

Bank 2 Lattice					
Lattice Location	Schematic Name	CPLD Bank	CPLD Pin	HDL Name	Physical Channel Name
AC12	Bank2_IO(82)	2	C5	cBank2ioD(4)	Bank2_PortD_DIO4
AC13	Bank2_IO(83)	2	C6	cBank2ioD(5)	Bank2_PortD_DIO5
AC14	Bank2_IO(84)	2	C7	cBank2ioD(6)	Bank2_PortD_DIO6
AC15	Bank2_IO(85)	2	C8	cBank2ioD(7)	Bank2_PortD_DIO7
AC16	Bank2_IO(86)	2	C9	cBank2ioE(0)	Bank2_PortE_DIO0
AC17	Bank2_IO(87)	2	D10	cBank2ioE(1)	Bank2_PortE_DIO1
AC18	Bank2_IO(88)	2	D11	cBank2ioE(2)	Bank2_PortE_DIO2
AC19	Bank2_IO(89)	2	D12	cBank2ioE(3)	Bank2_PortE_DIO3
AE19	Bank2_IO(90)	2	D4	cBank2ioE(4)	Bank2_PortE_DIO4
AE18	Bank2_IO(91)	2	D5	cBank2ioE(5)	Bank2_PortE_DIO5
AE17	Bank2_IO(92)	2	D6	cBank2ioE(6)	Bank2_PortE_DIO6
AE16	Bank2_IO(93)	2	D7	cBank2ioE(7)	Bank2_PortE_DIO7
AE15	Bank2_IO(94)	2	D8	cBank2ioF(0)	Bank2_PortF_DIO0
AE14	Bank2_IO(95)	2	D9	cBank2ioE(1)	Bank2_PortF_DIO0
AE13	Bank2_IO(96)	2	E10	cBank2ioE(2)	Bank2_PortF_DIO0
AE12	Bank2_IO(97)	2	E11	cBank2ioE(3)	Bank2_PortF_DIO0
AE11	Bank2_IO(98)	2	E6	cBank2ioE(4)	Bank2_PortF_DIO0
AE10	Bank2_IO(99)	2	E7	cBank2ioE(5)	Bank2_PortF_DIO0
AE9	Bank2_IO(100)	2	E8	cBank2ioE(6)	Bank2_PortF_DIO0
AE8	Bank2_IO(101)	2	E9	cBank2ioE(7)	Bank2_PortF_DIO0

Table 6. Connector 2 Connectivity to Bank 2 Prototyping Area

Connector J2					
J2 Pin	**Schematic Name**[4]	**Lattice Coordinate (Bank 2)**	**J2 Pin**	**Schematic Name**[5]	**Lattice Coordinate (Bank 2)**
1	Front2_IO(1)	A24	23	Front2_IO(23)	D24
2	Front2_IO(2)	A23	24	Front2_IO(24)	D23
3	Front2_IO(3)	A22	25	Front2_IO(25)	D22
4	Front2_IO(4)	A21	26	Front2_IO(26)	D21
5	Front2_IO(5)	A20	27	Front2_IO(27)	D20
6	Front2_IO(6)	A19	28	Front2_IO(28)	D19
7	Front2_IO(7)	A18	29	GND	GND
8	Front2_IO(8)	A17	30	Front2_IO(30)	D17
9	Front2_IO(9)	A16	31	Front2_IO(31)	D16
10	Front2_IO(10)	A15	32	Front2_IO(32)	D15
11	Front2_IO(11)	A14	33	Front2_IO(33)	D14
12	Front2_IO(12)	A13	34	Front2_IO(34)	D13
13	Front2_IO(13)	A12	35	Front2_IO(35)	D12
14	Front2_IO(14)	A11	36	Front2_IO(36)	D11
15	Front2_IO(15)	A10	37	Front2_IO(37)	D10
16	Front2_IO(16)	A9	38	Front2_IO(38)	D9
17	GND	GND	39	Front2_IO(39)	D8
18	Front2_IO(18)	A7	40	Front2_IO(40)	D7
19	Front2_IO(19)	A6	41	Front2_IO(41)	D6
20	Front2_IO(20)	A5	42	Front2_IO(42)	D5
21	Front2_IO(21)	A4	43	Front2_IO(43)	D4
22	Front2_IO(22)	A3	44	Front2_IO(44)	D3

4. In the silkscreen, these signals are marked IO2(Pin Number) for space reasons
5. In the silkscreen, these signals are marked IO2(Pin Number) for space reasons

Table 7. Miscellaneous Signals in Bank 2 Prototyping Area

Miscellaneous Signals			
Coordinate	**Signal**	**Coordinate**	**Signal**
A1-D1	BANK2_VCC	E1-AC1	GND
A25-D15	BANK2_VCC	B2-B24	GND
AD1	BANK2_VCC	E25-AC25	GND
AE1	BANK2_VCC	AD2-AD24	GND
AD25	BANK2_VCC	C24	GND
AE25	BANK2_VCC	C23	VCC (5 V)

Bank 3 Prototyping Area

Figure 1. Bank 3 Prototyping Area

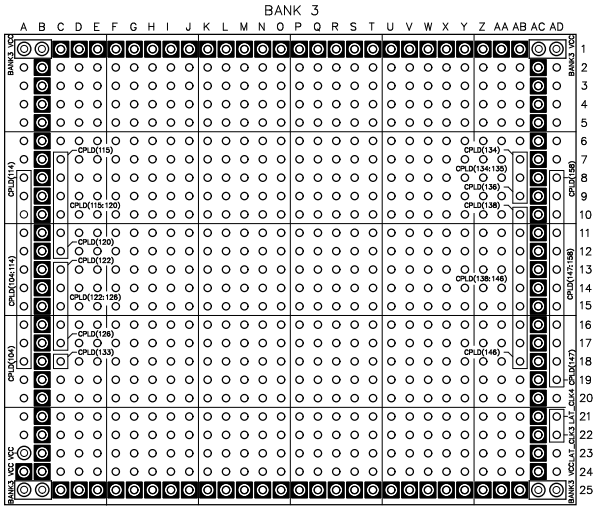


Table 8. CPLD Connectivity to Bank 3 Prototyping Area

Bank 3 Lattice					
Lattice Location	**Schematic Name**[6]	**CPLD Bank**	**CPLD Pin**	**HDL Name**	**Physical Channel Name**
A18	Bank3_IO(104)	3	C14	cBank3ioA(0)	Bank3_PortA_DIO0
A17	Bank3_IO(105)	3	C15	cBank3ioA(1)	Bank3_PortA_DIO1
A16	Bank3_IO(106)	3	D13	cBank3ioA(2)	Bank3_PortA_DIO2
A15	Bank3_IO(107)	3	D14	cBank3ioA(3)	Bank3_PortA_DIO3

6. In the silkscreen, these signals are marked as CPLD(Pin Number) for space reasons.

Bank 3 Lattice					
Lattice Location	Schematic Name	CPLD Bank	CPLD Pin	HDL Name	Physical Channel Name
A14	Bank3_IO(108)	3	D15	cBank3ioA(4)	Bank3_PortA_DIO4
A13	Bank3_IO(109)	3	D16	cBank3ioA(5)	Bank3_PortA_DIO5
A12	Bank3_IO(110)	3	E12	cBank3ioA(6)	Bank3_PortA_DIO6
A11	Bank3_IO(111)	3	E13	cBank3ioA(7)	Bank3_PortA_DIO7
A10	Bank3_IO(112)	3	E14	cBank3ioB(0)	Bank3_PortB_DIO0
A9	Bank3_IO(113)	3	E15	cBank3ioB(1)	Bank3_PortB_DIO1
A8	Bank3_IO(114)	3	E16	cBank3ioB(2)	Bank3_PortB_DIO2
C7	Bank3_IO(115)	3	F11	cBank3ioB(3)	Bank3_PortB_DIO3
C8	Bank3_IO(116)	3	F12	cBank3ioB(4)	Bank3_PortB_DIO4
C9	Bank3_IO(117)	3	F13	cBank3ioB(5)	Bank3_PortB_DIO5
C10	Bank3_IO(118)	3	F14	cBank3ioB(6)	Bank3_PortB_DIO6
C11	Bank3_IO(119)	3	F15	cBank3ioB(7)	Bank3_PortB_DIO7
C12	Bank3_IO(120)	3	F16	cBank3ioC(0)	Bank3_PortC_DIO0
C13	Bank3_IO(122)	3	G12	cBank3ioC(1)	Bank3_PortC_DIO1
C14	Bank3_IO(123)	3	G13	cBank3ioC(2)	Bank3_PortC_DIO2
C15	Bank3_IO(124)	3	G14	cBank3ioC(3)	Bank3_PortC_DIO3
C16	Bank3_IO(125)	3	G15	cBank3ioC(4)	Bank3_PortC_DIO4
C17	Bank3_IO(126)	3	G16	cBank3ioC(5)	Bank3_PortC_DIO5
C18	Bank3_IO(133)	3	J13	cBank3ioC(6)	Bank3_PortC_DIO6
AB7	Bank3_IO(134)	3	J14	cBank3ioD(0)	Bank3_PortD_DIO0
AB8	Bank3_IO(135)	3	J15	cBank3ioD(1)	Bank3_PortD_DIO1
AB9	Bank3_IO(136)	3	J16	cBank3ioD(2)	Bank3_PortD_DIO2
AB10	Bank3_IO(138)	3	K12	cBank3ioD(3)	Bank3_PortD_DIO3
AB11	Bank3_IO(139)	3	K13	cBank3ioD(4)	Bank3_PortD_DIO4
AB12	Bank3_IO(140)	3	K14	cBank3ioD(5)	Bank3_PortD_DIO5

Bank 3 Lattice					
Lattice Location	Schematic Name	CPLD Bank	CPLD Pin	HDL Name	Physical Channel Name
AB13	Bank3_IO(141)	3	K15	cBank3ioD(6)	Bank3_PortD_DIO6
AB14	Bank3_IO(142)	3	K16	cBank3ioD(7)	Bank3_PortD_DIO7
AB15	Bank3_IO(143)	3	L11	cBank3ioE(0)	Bank3_PortE_DIO0
AB16	Bank3_IO(144)	3	L12	cBank3ioE(1)	Bank3_PortE_DIO1
AB17	Bank3_IO(145)	3	L13	cBank3ioE(2)	Bank3_PortE_DIO2
AB18	Bank3_IO(146)	3	L14	cBank3ioE(3)	Bank3_PortE_DIO3
AD19	Bank3_IO(147)	3	L15	cBank3ioE(4)	Bank3_PortE_DIO4
AD18	Bank3_IO(148)	3	L16	cBank3ioE(5)	Bank3_PortE_DIO5
AD17	Bank3_IO(149)	3	M13	cBank3ioE(6)	Bank3_PortE_DIO6
AD16	Bank3_IO(150)	3	M14	cBank3ioE(7)	Bank3_PortE_DIO7
AD15	Bank3_IO(151)	3	M15	cBank3ioF(0)	Bank3_PortF_DIO0
AD14	Bank3_IO(152)	3	M16	cBank3ioF(1)	Bank3_PortF_DIO1
AD13	Bank3_IO(153)	3	N13	cBank3ioF(2)	Bank3_PortF_DIO2
AD12	Bank3_IO(154)	3	N14	cBank3ioF(3)	Bank3_PortF_DIO3
AD11	Bank3_IO(155)	3	N15	cBank3ioF(4)	Bank3_PortF_DIO4
AD10	Bank3_IO(156)	3	N16	cBank3ioF(5)	Bank3_PortF_DIO5
AD9	Bank3_IO(157	3	P14	cBank3ioF(6)	Bank3_PortF_DIO6
AD8	Bank3_IO(158)	3	P15	cBank3ioF(7)	Bank3_PortF_DIO7

Table 9. Miscellaneous Signals in Bank 3 Prototyping Area

Miscellaneous Signals			
Coordinate	Signal	Coordinate	Signal
A1	BANK3_VCC	C1-AB1	GND
B1	BANK3_VCC	B2-B24	GND
A25	BANK3_VCC	C25-AB25	GND
B25	BANK3_VCC	AC2-AC24	GND

Miscellaneous Signals			
Coordinate	**Signal**	**Coordinate**	**Signal**
AC1	BANK3_VCC	A24	GND
AD1	BANK3_VCC	A23	VCC (5 V)
AC25	BANK3_VCC	AD21	LAT_CLK4
AD25	BANK3_VCC	AD22	LAT_CLK3

Bank 4 Prototyping Area

Figure 1. Bank 4 Prototyping Area

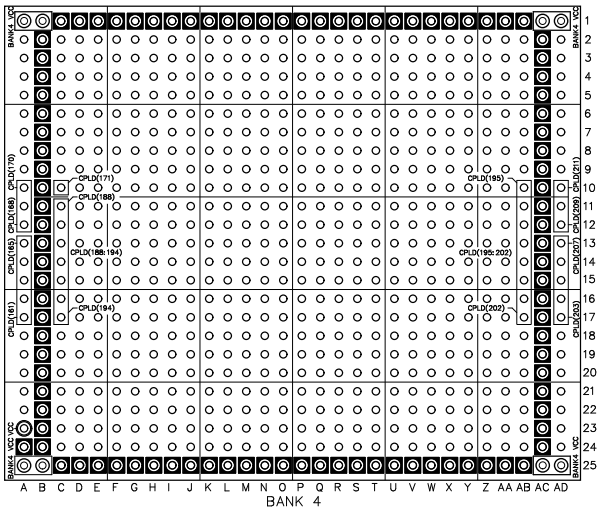


Table 10. CPLD Connectivity to Bank 4 Prototyping Area

Bank 4 Lattice					
Lattice Location	**Schematic Name**[7]	**CPLD Bank**	**CPLD Pin**	**HDL Name**	**Physical Channel Name**
A17	Bank4_IO(161)	4	M10	cBank4ioA(0)	Bank4_PortA_DIO0
A16	Bank4_IO(162)	4	M11	cBank4ioA(1)	Bank4_PortA_DIO1
A15	Bank4_IO(163)	4	M12	cBank4ioA(2)	Bank4_PortA_DIO2
A14	Bank4_IO(164)	4	M6	cBank4ioA(3)	Bank4_PortA_DIO3
A13	Bank4_IO(165)	4	M7	cBank4ioA(4)	Bank4_PortA_DIO4
A12	Bank4_IO(168)	4	N10	cBank4ioA(5)	Bank4_PortA_DIO5

7. In the silkscreen, these signals are marked as CPLD(Pin Number) for space reasons.

Bank 4 Lattice					
Lattice Location	Schematic Name	CPLD Bank	CPLD Pin	HDL Name	Physical Channel Name
A11	Bank4_IO(169)	4	N11	cBank4ioA(6)	Bank4_PortA_DIO6
A10	Bank4_IO(170)	4	N12	cBank4ioA(7)	Bank4_PortA_DIO7
C10	Bank4_IO(171)	4	N5	cBank4ioB(0)	Bank4_PortB_DIO0
C11	Bank4_IO(188)	4	R11	cBank4ioB(1)	Bank4_PortB_DIO1
C12	Bank4_IO(189)	4	R12	cBank4ioB(2)	Bank4_PortB_DIO2
C13	Bank4_IO(190)	4	R13	cBank4ioB(3)	Bank4_PortB_DIO3
C14	Bank4_IO(191)	4	R14	cBank4ioB(4)	Bank4_PortB_DIO4
C15	Bank4_IO(192)	4	R16	cBank4ioB(5)	Bank4_PortB_DIO5
C16	Bank4_IO(193)	4	R3	cBank4ioB(6)	Bank4_PortB_DIO6
C17	Bank4_IO(194)	4	R4	cBank4ioB(7)	Bank4_PortB_DIO7
AB10	Bank4_IO(195)	4	R5	cBank4ioC(0)	Bank4_PortC_DIO0
AB11	Bank4_IO(196)	4	R6	cBank4ioC(1)	Bank4_PortC_DIO1
AB12	Bank4_IO(197)	4	R7	cBank4ioC(2)	Bank4_PortC_DIO2
AB13	Bank4_IO(198)	4	R8	cBank4ioC(3)	Bank4_PortC_DIO3
AB14	Bank4_IO(199)	4	R9	cBank4ioC(4)	Bank4_PortC_DIO4
AB15	Bank4_IO(200)	4	T10	cBank4ioC(5)	Bank4_PortC_DIO5
AB16	Bank4_IO(201)	4	T11	cBank4ioC(6)	Bank4_PortC_DIO6
AB17	Bank4_IO(202)	4	T12	cBank4ioC(7)	Bank4_PortC_DIO7
AD17	Bank4_IO(203)	4	T13	cBank4ioD(0)	Bank4_PortD_DIO0
AD16	Bank4_IO(204)	4	T15	cBank4ioD(1)	Bank4_PortD_DIO1
AD15	Bank4_IO(205)	4	T2	cBank4ioD(2)	Bank4_PortD_DIO2
AD14	Bank4_IO(206)	4	T4	cBank4ioD(3)	Bank4_PortD_DIO3
AD13	Bank4_IO(207)	4	T5	cBank4ioD(4)	Bank4_PortD_DIO4
AD12	Bank4_IO(209)	4	T7	cBank4ioD(5)	Bank4_PortD_DIO5
AD11	Bank4_IO(210)	4	T8	cBank4ioD(6)	Bank4_PortD_DIO6

Bank 4 Lattice					
Lattice Location	**Schematic Name**	**CPLD Bank**	**CPLD Pin**	**HDL Name**	**Physical Channel Name**
AD10	Bank4_IO(211)	4	T9	cBank4ioD(7)	Bank4_PortD_DIO7

Table 11. Miscellaneous Signals in Bank 4 Prototyping Area

Miscellaneous Signals			
Coordinate	**Signal**	**Coordinate**	**Signal**
A1	BANK4_VCC	AD25	BANK4_VCC
B1	BANK4_VCC	C1-AB1	GND
A25	BANK4_VCC	B2-B24	GND
B25	BANK4_VCC	C25-AB25	GND
AC1	BANK4_VCC	AC2-AC24	GND
AD1	BANK4_VCC	A24	GND
AC25	BANK4_VCC	A23	VCC (5 V)

RTI Prototyping Area

Figure 1. RTI Prototyping Area

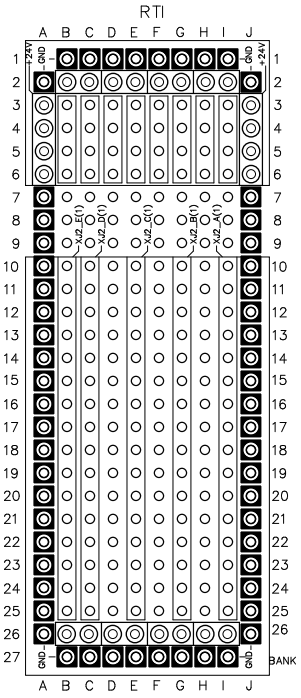


Table 12. Connectivity of XJ2 Connector to RTI Prototyping Area

Connector XJ2									
XJ2 pin	Lattice Coordinate (RTI)	XJ2 pin	Lattice Coordinate (RTI)	XJ2 pin	Lattice Coordinate (RTI)	XJ2 pin	Lattice Coordinate (RTI)	XJ2 pin	Lattice Coordinate (RTI)
A1	I10	B1	G10	C1	E10	D1	C10	E1	B10
A2	I11	B2	G11	C2	E11	D2	C11	E2	B11
A3	GND	B3	GND	C3	GND	D3	GND	E3	GND
A4	I12	B4	G12	C4	E12	D4	C12	E4	B12
A5	I13	B5	G13	C5	E13	D5	C13	E5	B13
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND
A7	I14	B7	G14	C7	E14	D7	C14	E7	B14
A8	I15	B8	G15	C8	E15	D8	C15	E8	B15
A9	GND	B9	GND	C9	GND	D9	GND	E9	GND
A10	I16	B10	G16	C10	E16	D10	C16	E10	B16
A11	I17	B11	G17	C11	E17	D11	C17	E11	B17
A15	I18	B15	G18	C15	E18	D15	C18	E15	B18
A16	I19	B16	G19	C16	E19	D16	C19	E16	B19
A17	GND	B17	GND	C17	GND	D17	GND	E17	GND
A18	I20	B18	G20	C18	E20	D18	C20	E18	B20
A19	I21	B19	G21	C19	E21	D19	C21	E19	B21
A20	GND	B20	GND	C20	GND	D20	GND	E20	GND
A21	I22	B21	G22	C21	E22	D21	C22	E21	B22
A22	I23	B22	G23	C22	E23	D22	C23	E22	B23
A23	GND	B23	GND	C23	GND	D23	GND	E23	GND
A24	I24	B24	G24	C24	E24	D24	C24	E24	B24
A25	I25	B25	G25	C25	E25	D25	C25	E25	B25

Table 13. Connectivity of XJ3 Connector to RTI Prototyping Area

Connector XJ3	
XJ3 Pin	Lattice Coordinates (RTI)
A	I(3-6)
B	H(3-6)
C	G(3-6)
D	F(3-6)
E	E(3-6)
F	D(3-6)

Connector XJ3	
XJ3 Pin	**Lattice Coordinates (RTI)**
G	C(3-6)
H	B(3-6)

Table 14. RTI Miscellaneous Signals

Miscellaneous Signals			
Coordinate	**Signal**	**Coordinate**	**Signal**
B1-I1	GND	J3-J6	24 V
A2	GND	A7-A26	GND
B2-C2	3.3 V	J7-J26	GND
D2-E2	Bank 2 VCC	D26-E26	Bank 2 VCC
F2-G2	Bank 3 VCC	F26-G26	Bank 3 VCC
H2-I2	Bank 4 VCC	H26-I26	Bank 4 VCC
A3-A6	24 V	B27-I27	GND

CPLD Pins

Table 15. Miscellaneous Connections to the CPLD

Miscellaneous Pins				
Schematic Name	**CPLD Bank**	**CPLD Pin**	**Pin Name**	**Notes**
Bank2_IO(77)	2	C10	aTFM_Lattice	
Bank2_IO(76)	2	B9	aTTM_Lattice	
Bank2_IO(63)	2	B1	unused	
CPLD_CLK1	1	H5	Clk	System clock for the design.
LED_Red_0	1	L1	cPowerGreen	LED signal.
LED_Green_0	1	L3	cPowerRed	LED signal.
LED_Red_1	1	L2	cReadyGreen	LED signal.
LED_Green_1	1	L4	cReadyRed	LED signal.

Miscellaneous Pins				
Schematic Name	**CPLD Bank**	**CPLD Pin**	**Pin Name**	**Notes**
CPLDESET#	1	K4	aReset_n	Module Reset.

Table 16. Rotary Switch Connectivity to the CPLD

Rotary Switch					
SW1 pin	**Schematic Name**	**CPLD Bank**	**CPLD Pin**	**HDL Name**	**Physical Channel Name**
1	Switch(0)	3	H16	aSwitch(0)	NI.RotarySwitch
2	Switch(1)	3	H15	aSwitch(1)	NI.RotarySwitch
4	Switch(2)	3	H14	aSwitch(2)	NI.RotarySwitch
8	Switch(3)	3	H13	aSwitch(3)	NI.RotarySwitch
C	Bank3_VCC				

Table 17. SI 5356 Clock Generator Connectivity to the CPLD

SI5356 Clock Generator Interface				
SI5356 pin	**Schematic Name**	**CPLD Bank**	**CPLD Pin**	**HDL Name**
8	CLK_INT	1	F5	unused
18	CPLD_CLK2	1	J5	unused
14	CPLD_CLK3	3	H12	unused
10	CPLD_CLK4	3	J12	unused
12	SCL_HDR	1	F6	unused
19	SDA_HDR	1	G1	unused
5	SSC_DIS	1	K5	unused

Table 18. Temperature Sensors Connectivity to the CPLD

Temperature Sensors							
Pin Number on Sensor							
Sensor 1	Sensor 2	Sensor 3	Sensor 4	Schematic Name	CPLD Bank	CPLD Pin	HDL Name
	1	1		SPI0_CLK	1	C2	aSpi0Clk
	2	2		SPI0_MISO	1	C3	aSpi0Miso
	3	3		SPI0_MOSI	1	D1	aSpi0Mosi
	4			SPI0_CS#(0)	1	D2	aSpi0Ss(0)
		4		SPI0_CS#(1)	1	D3	aSpi0Ss(1)
	6	6		L0_CT	1	F1	aL0Ct
	5	5		L0_INT	1	F2	aL0Int
1			1	SPI1_CLK	1	E1	aSpi1Clk
2			2	SPI1_MISO	1	E2	aSpi1Miso
3			3	SPI1_MOSI	1	E3	aSpi1Mosi
4				SPI1_CS#(0)	1	E4	aSpi1Ss(0)
			4	SPI1_CS#(1)	1	E5	aSpi1Ss(1)
6			6	L1_CT	1	F3	aL1Ct
5			5	L1_INT	1	F4	aL1Int

Design Standards and Compatibility

Switch Load and Signal Conditioning Module Design Specifications Version	1.0
SLSC Compliance Level[8]	2
Rear I/O Compatibility Category	User-defined

8. SLSC-12101 may be upgraded to Level 1 by implementing Fully Compatible Rear I/O.

DC and AC Characteristics

Parameter	Minimum	Typical	Maximum	Notes
CPLD Clock Frequency. U6	40 MHz − 100 ppm	40 MHz	40 MHz + 100 ppm	Using the SG-310 Oscillator.
24 V	20.4 V	24 V	27.6 V	Supplied by the SLSC chassis.
Bank 1 VCC	3.135 V	3.3 V	3.465 V	Supplied by the SLSC chassis.
Bank 2-4 VCC, configured for 1.2 V	1.17 V	1.2 V	1.23 V	—
Bank 2-4 VCC, configured for 1.5 V	1.463 V	1.5 V	1.538 V	—
Bank 2-4 VCC, configured for 1.8 V	1.755 V	1.8 V	1.845 V	—
Bank 2-4 VCC, configured for 2.5 V	2.438 V	2.5 V	2.563 V	—
Bank 2-4 VCC, configured for 3.3 V	3.218 V	3.3 V	3.383 V	—
Bank 1 Maximum I			400 mA	This is the maximum current that can be withdrawn from the backplane. You can use W6 to measure the current used by your design.
Bank 2-4 Maximum I			2 A	For all voltages.
24 V Maximum I			2 A	This is the

Parameter	Minimum	Typical	Maximum	Notes
				maximum current that can be withdrawn from the backplane. You can use W1 to measure the current used by your design.
XJ3 Maximum Current			8 A	Per blade.
XJ3 Maximum Voltage	-60 V		60 V	DC limit. Additional limitations are given in the ***Switch Load and Signal Conditioning Module Design Specifications*** document.
XJ2 Maximum Current			1 A	Per pin.
XJ2 Maximum Voltage	-32 V		32 V	DC limit. Additional limitations are given in the ***Switch Load and Signal Conditioning Module Design Specifications*** document.
J10, J11 Maximum Current			0.4 mA	Limit per pin. The limit is driven by trace width.
J10, J11 Maximum Voltage	-60 V		60 V	DC limit.

Parameter	Minimum	Typical	Maximum	Notes
DIO V OH	2.4 V			Values for the default CPLD program using 3.3 V-LVTTL and -4 mA.
DIO V OL			0.45 V	Values for the default CPLS program using 3.3 V-LVTTL and 4 mA.
DIO V IH	1.7 V		4.0 V	Values for the default CPLD program using 3.3 V-LVTTL.
DIO V IL	-0.5 V		0.8 V	Values for the default CPLD program using 3.3 V-LVTTL.
DIO Maximum Current			25 mA	Absolute maximum rating.

Power Requirements

If the SLSC-12101 is modified, you must ensure it meets all the power requirements in the ***Switch Load and Signal Conditioning Module Design Specifications***.

Maximum current drawn from backplane, without module customization (Typical)	
3.3 V	50 mA
24 V	30 mA
Power dissipation (Typical)	900 mW

Maximum allowed continuous power dissipation (Limited by specification)	50 W

Thermal Considerations

All components on the SLSC-12101 are rated for an ambient temperature of at least 85 °C. The components do not exceed 85 °C when the module is dissipating the maximum allowed power using resistors spread out over the prototyping areas. However, large components or grouped placement of very hot components may negatively affect airflow and heat dissipation, resulting in higher component temperatures.

Whenever possible, thorough thermal testing should be conducted in order to ensure the components remain within proper operational temperature ranges. Because chassis airflow characteristics may vary greatly from slot to slot, module testing should be repeated in a variety of slots.

Physical Characteristics

SLSC slots	1
Dimensions	175 mm × 31 mm × 336 mm (6.89 in × 1.19 in × 13.21 in)
Weight	283 g (10.0 oz)
Front I/O Connectors	2x high-density 44-position DSUB
Rear I/O Connectors	1x 110-pin Hard Metric Type A, 1x 8-blade Universal Power Module (UPM), capable of implementing Fully Compatible Rear I/O

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Operating vibration, random	5 to 500 Hz, 0.3 g RMS
Non-operating vibration, random	5 to 500 Hz, 2.4 g RMS

Safety Guidelines

Measurement Category	I

Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as ***MAINS*** voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.

Caution Do not connect the SLSC-12101 to signals or use for measurements within Measurement Categories II, III, or IV.

Note Measurement Categories CAT I and CAT O are equivalent. These test and measurement circuits are for other circuits not intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

Safety

This product is designed to meet the requirements of the following electrical

equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Environmental

Module operating temperature	0 °C to 85 °C [9]

Storage temperature range	-40 °C to 85 °C
Relative humidity range, operating	10% to 90%, noncondensing
Relative humidity range, storage	5% to 95%, noncondensing
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient)
Pollution Degree	2

Indoor use only.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

9. The chassis internal ambient temperature may reach 85 °C with all slots at the maximum allowed power dissipation.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)
- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.