PXIe-6595 Specifications

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PXIe-6595 Specifications

These specifications apply to the PXIe-6595 when used in the Semiconductor Test System (STS).

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Typical*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C
- Installed in chassis with slot cooling capacity ≥58 W

PORT 0, PORT 1

Data rate	500 Mb/s to 32.75 Gb/s

Connector	Ardent Concepts TR40 16×2
Number of channels	8 RX/TX (GTY)

MGT TX± Channels[1]

Differential output voltage[2]	
Minimum	390 mV pk-pk into 100 Ω, nominal
Maximum	1040 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

MGT RX± Channels

Differential and single-ended voltages must meet all the following conditions:

Differential voltage	$V_{CM\_TRIM} + V_{DIFF} / 4 \leq 1.2$ V $V_{CM\_TRIM} - V_{DIFF} / 4 \geq -0.4$ V $150 \text{ mV} \leq V_{DIFF} \leq 1.2$ V
Single-ended voltage	$-8 \text{ V} \leq V_{SE} \leq 8$ V

where V_{CM_TRIM} is the common mode voltage[3] configured on the MGT RX± transceivers, V_{DIFF} is the differential peak-peak voltage, and V_{SE} is the single-ended

voltage.

Recommended common mode voltage (V_{CM_TRIM})	800 mV
Differential input resistance	100 Ω, nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

MGT Reference Clock Generator

Supported output frequencies	60.000 MHz to 385.714 MHz 400.000 MHz to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHz to 771.428 MHz 800 MHz
Locking resources	PXIe_CLK100 REF/CLK IN
Available MGT Reference Clocks	4

CLK OUT

Connector type	SMA

Coupling	AC
Output impedance	50 Ω, nominal
Supported output frequencies	2.344 MHz to 385.714 MHz 400.000 MHz to 450.000 MHz 480.000 MHz to 675.000 MHz 685.714 MHz to 771.428 MHz 800.000 MHz to 900.000 MHz 960.000 MHz to 1000.000 MHz
Output voltage range	0.61 V pk-pk to 1.04 V pk-pk

REF/CLK IN

Connector type	SMA
Input coupling	AC
Input impedance	50 Ω
Frequency range	10 MHz to 300 MHz
Input voltage range	0.3 V pk-pk to 4 V pk-pk

Absolute maximum voltage	5 V pk-pk AC
Duty cycle	45% to 55%

Reconfigurable FPGA

Kintex Ultrascale+	15P
LUTs	523,000
DSP48 slices (25 × 18 multiplier)	1,968
Embedded Block RAM	34.6 Mb
Timebase reference sources	PXI Express 100 MHz (PXI_CLK100)
Data transfers	DMA, interrupts, programmed I/O, MGTs
Number of DMA channels	60

Onboard DRAM

Memory size	8 GB (2 banks of 4 GB)
DRAM clock rate	1333 MHz

Physical bus width	64 bit
LabVIEW FPGA DRAM clock rate	333 MHz
LabVIEW FPGA DRAM bus width	512 bits per bank
Maximum theoretical data rate	42.7 GB/s (21.3 GB/s per bank)

Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	3.3 A
Maximum total power	40 W

Physical

Dimensions (not including connectors)	2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	416 g (14.7 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[4]
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}