PCI-5421 Specifications

2025-03-10

Contents

PCI-5421 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are ***Nominal*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 0 °C to 55 °C
- Analog filter enabled
- Interpolation set to maximum allowed factor for a given sample rate
- Signals terminated with 50 Ω
- Direct path set to 1 Vpk-pk
- Low-gain amplifier path set to 2 Vpk-pk
- High-gain amplifier path set to 12 Vpk-pk
- Sample Clock set to 100 MS/s

Typical specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 23 ±5 °C

PCI-5421 Pinout

Use the pinout to connect to terminals on the PCI-5421.

Figure 1. PCI-5421 DDC 68-pin Connector Pinout

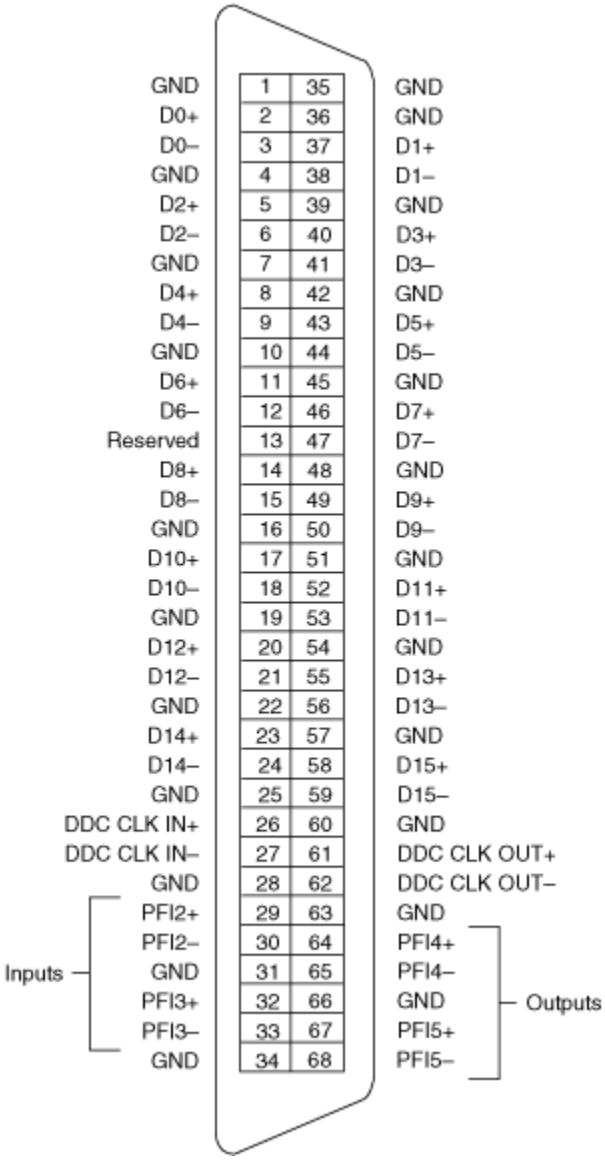


Table 1. Signal Descriptions

Signal Name	Type	Description
D<0..15>	Output	Digital pattern outputs. The 16-bit digital representation of the analog waveform is available on these output pins as digital pattern outputs. This

Signal Name	Type	Description
		data is available directly from the memory after several Sample clock pipeline delays. The digital pattern outputs are standard LVDS output levels. All data bits change on the falling edge of the DDC CLK OUT.
DDC CLK IN	Input	These lines are used as a source for an external Sample clock. You can feed a LVDS level clock to this line with a maximum frequency of the signal generator.
DDC CLK OUT	Output	The Sample clock is always routed to the DDC CLK OUT line of the DDC front panel connector when the digital pattern is enabled.
Ground	—	Digital ground.
PFI<2..3> (Inputs)	Input	These PFI lines can accept a trigger from an external source that can start or step through waveform generation. You can select this functionality on the NI 5421 through the software.
PFI<4:5>	Output	These PFI lines can route out a signal from Marker events or the Out Start trigger.
Reserved	—	Reserved for future use. Do not connect signals to this line.

CH 0 Analog Output

Number of channels	1

Connector type	SMB jack

Output Voltage

Full-scale voltage	
Main output path[1][1]	12.00 V pk-pk to 5.64 mV pk-pk into a 50 Ω load
Direct output path[2][2]	1.000 V pk-pk to 0.707 V pk-pk
DAC resolution	16 bits

Amplitude and Offset

Table 2. Amplitude Range[3]

Path	**Load**	**Amplitude (V pk-pk)**	
		Minimum	**Maximum**
Direct	50 Ω	0.707	1.00
	1 kΩ	1.35	1.91
	Open	1.41	2.00
Low-gain amplifier	50 Ω	0.00564	2.00
	1 kΩ	0.0107	3.81
	Open	0.0113	4.00
High-gain	50 Ω	0.0338	12.0

1. When the main output path is selected, either the low-gain amplifier or the high-gain amplifier is used, depending on the value of the Gain property or NIFGEN_ATTR_GAIN attribute.
2. The direct path is optimized for intermediate frequency (IF) applications.
3. Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used. NI-FGEN compensates for user-specified resistive loads.

Path	Load	Amplitude (V pk-pk)	
		Minimum	Maximum
amplifier	1 kΩ	0.0644	22.9
	Open	0.0676	24.0

Amplitude resolution	<0.06% (0.004 dB) of ***Amplitude Range***
Offset range[4]	Span of ±25% of ***Amplitude Range*** with increments <0.0014% of ***Amplitude Range***

Accuracy

Table 3. DC Accuracy[5]

Path	DC Accuracy	
	±10 °C of Self-Calibration Temperature	**0 °C to 55 °C**
Low-gain amplifier	±0.2% of ***Amplitude Range*** ± 0.05% of ***Offset*** ± 500 µV	±0.4% of ***Amplitude Range*** ± 0.05% of ***Offset*** ± 1 mV
High-gain amplifier		
Direct	±0.2% ***Amplitude Range***	±0.4% ***Amplitude Range***

DC offset error[6]	±30 mV

4. Offset range is not available on the direct path.
5. All paths are calibrated for amplitude and gain errors. The low-gain and high-gain amplifier paths are also calibrated for offset errors. DC accuracy is calibrated into a high-impedance load. ***Amplitude Range*** is defined as two times the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, DC accuracy is calculated by the following equation: ±0.2% * (16 V) ± 0.05% * (1.5 V) ± 500µV = ±33.25 mV

AC amplitude accuracy[7]	(+2.0% + 1 mV), (-1.0% - 1 mV) (+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical

Output

Output impedance	Software-selectable: 50 Ω or 75 Ω, nominal
Load impedance compensation	Output amplitude is compensated for user-specified load impedances
Output coupling	DC
Output enable	Software-selectable[8]
Maximum output overload	CH 0 can be connected to a 50 Ω, ±12 V (±8 V for the direct path) source without sustaining any damage.[9]
Waveform summing	Supported[10]

Frequency and Transient Response

Bandwidth[11][11]	43 MHz

6. Within 0 °C to 55 °C.
7. With a 50 kHz sine wave and terminated with high impedance.
8. When the output path is disabled, CH 0 is terminated to ground with a 1 W resistor with a value equal to the selected output impedance.
9. No damage occurs if CH 0 is shorted to ground indefinitely.
10. The output terminals of multiple PCI-5421 waveform generators can be connected directly together.

Digital interpolation filter[12]	Software-selectable: Finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.
Analog filter[13]	Software-selectable: 7-pole elliptical filter
Passband flatness [14]	
Direct path	-0.4 dB to +0.6 dB, 100 Hz to 40 MHz
Low-gain amplifier path	-1.0 dB to +0.5 dB, 100 Hz to 20 MHz
High-gain amplifier path	-1.2 dB to +0.5 dB, 100 Hz to 20 MHz
Pulse response[15]	
Direct path	
Rise/fall time	<5 ns
Aberration	<10%, typical
Low-gain amplifier path	
Rise/fall time	<8 ns
Aberration	<5%, typical

11. Measured at -3 dB.
12. The digital filter is not available for use for Sample Clock rates below 10 MS/s. Refer to Effective Sample Rate for more information about the effect of interpolation on sample rates.
13. Available on low-gain amplifier and high-gain amplifier paths.
14. With respect to 50 kHz.

High-gain amplifier path	
Rise/fall time	<10 ns
Aberration	<5%, typical

Figure 2. Normalized Passband Flatness, Direct Path

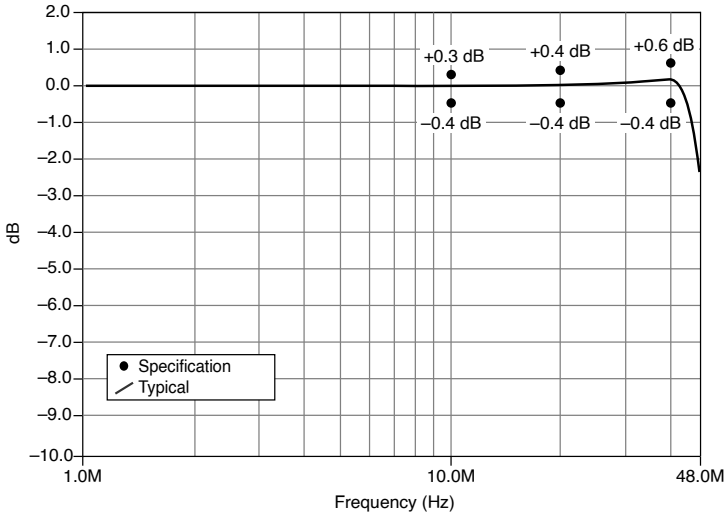
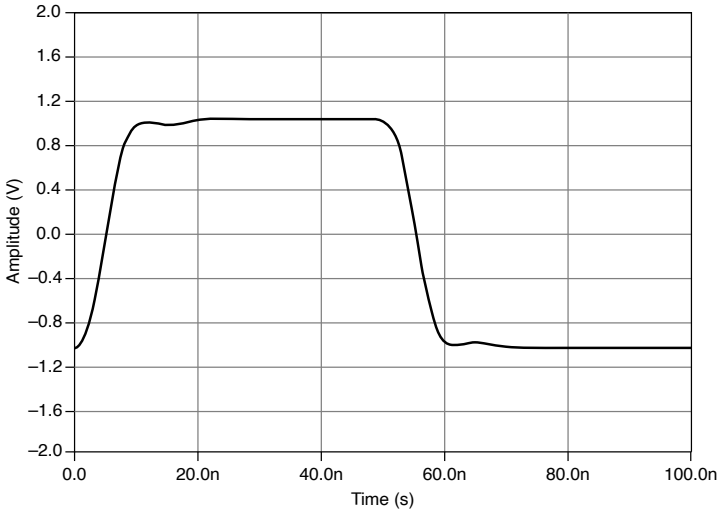


Figure 3. Pulse Response, Low-Gain Amplifier Path 50 Ω Load



Suggested Maximum Frequencies for Common Functions

Suggested maximum frequencies[16][16]

15. Analog filter and digital interpolation filter disabled.

Direct path	
Sine	43 MHz
Square	Not recommended
Ramp	Not recommended
Triangle	Not recommended
Low-gain amplifier path	
Sine	43 MHz
Square	25 MHz
Ramp	5 MHz
Triangle	5 MHz
High-gain amplifier path	
Sine	43 MHz
Square	12.5 MHz

16. Disable the analog filter and the digital interpolation filter for square, ramp, and triangle functions. The minimum frequency is <1 mHz. The value depends on memory size and instrument configuration.

Ramp	5 MHz
Triangle	5 MHz

Spectral Characteristics

Table 4. Spurious-Free Dynamic Range (SFDR) with Harmonics[17]

Frequency	SFDR with Harmonics (dB), Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
1 MHz	70	65	66
5 MHz			58
10 MHz			52
20 MHz	63	64	49
30 MHz	57	60	43
40 MHz	48	53	39
50 MHz			—
60 MHz	47	52	
70 MHz			
80 MHz	41		

Table 5. Spurious-Free Dynamic Range (SFDR) without Harmonics[]

Frequency	SFDR without Harmonics (dB), Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
1 MHz	84	79	76
5 MHz			
10 MHz	79		

17. At amplitude of -1 dBFS and measured from DC to 100 MHz. All values include aliased harmonics. Dynamic range is defined as the difference between the carrier level and the largest spur.

Frequency	SFDR without Harmonics (dB), Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
20 MHz			
30 MHz	72	70	67
40 MHz	47	57	54
50 MHz		52	—
60 MHz	46	51	
70 MHz			
80 MHz	40		

Table 6. Average Noise Density[18], Direct Path

Amplitude Range		Average Noise Density, Typical		
		$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
1.00 V pk-pk	4.0 dBm	19.9	-141	-145

Table 7. Average Noise Density[], Low-Gain Amplifier Path

Amplitude Range		Average Noise Density, Typical		
		$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
0.06 V pk-pk	-20.5 dBm	1.3	-148	-144
0.10 V pk-pk	-16.0 dBm	2.2		
0.40 V pk-pk	-4.0 dBm	8.9		
1.00 V pk-pk	4.0 dBm	22.3	-140	
2.00 V pk-pk	10.0 dBm	44.6	-134	

18. Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor.

Table 8. Average Noise Density[], High-Gain Amplifier Path

Amplitude Range		Average Noise Density, Typical		
		$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
4.00 V pk-pk	16.0 dBm	93.8	-128	-144
12.00 V pk-pk	25.6 dBm	281.5	-118	

Signal to Noise and Distortion (SINAD)[19]

All values are typical.

Direct path	
1 MHz	64 dB
10 MHz	61 dB
20 MHz	57 dB
30 MHz	60 dB
40 MHz	60 dB
43 MHz	58 dB
Low-gain amplifier path	
1 MHz	66 dB

19. Amplitude -1 decibel full scale (dBFS). Measured from DC to 50 MHz. SINAD at low amplitudes is limited by a -148 dBm/Hz noise floor.

10 MHz	60 dB
20 MHz	56 dB
30 MHz	62 dB
40 MHz	62 dB
43 MHz	60 dB
High-gain amplifier path	
1 MHz	63 dB
10 MHz	47 dB
20 MHz	42 dB
30 MHz	62 dB
40 MHz	62 dB
43 MHz	55 dB

Spurious-Free Dynamic Range (SFDR)

All values are typical and include aliased harmonics. Dynamic range is defined as the difference between the carrier level and the largest spur.

SFDR with harmonics[20]	
Direct path	
1 MHz	76 dB
10 MHz	68 dB
20 MHz	60 dB
30 MHz	73 dB
40 MHz	76 dB
43 MHz	78 dB
Low-gain amplifier path	
1 MHz	71 dB
10 MHz	64 dB
20 MHz	57 dB
30 MHz	73 dB
40 MHz	73 dB

20. Amplitude -1 dBFS. Measured from DC to 50 MHz. Also called harmonic distortion. SFDR with harmonics at low amplitudes is limited by a -148 dBm/Hz noise floor.

43 MHz	75 dB
High-gain amplifier path	
1 MHz	58 dB
10 MHz	47 dB
20 MHz	42 dB
30 MHz	74 dB
40 MHz	74 dB
43 MHz	59 dB
SFDR without harmonics[21]	
Direct path	
1 MHz	87 dB
10 MHz	86 dB
20 MHz	79 dB
30 MHz	72 dB

21. Amplitude -1 dBFS. Measured from DC to 50 MHz. SFDR without harmonics at low amplitudes is limited by a -148 dBm/Hz noise floor.

40 MHz	75 dB
43 MHz	77 dB
Low-gain amplifier path	
1 MHz	90 dB
10 MHz	88 dB
20 MHz	88 dB
30 MHz	72 dB
40 MHz	72 dB
43 MHz	74 dB
High-gain amplifier path	
1 MHz	90 dB
10 MHz	90 dB
20 MHz	88 dB
30 MHz	73 dB

40 MHz	73 dB
43 MHz	59 dB

Total Harmonic Distortion (THD)

THD[22] **(0 °C to 40 °C)**	
Direct path	
20 kHz	-77 dBc, typical
1 MHz	-75 dBc, typical
5 MHz	-68 dBc
10 MHz	-65 dBc
20 MHz	-55 dBc
30 MHz	-50 dBc
40 MHz	-47 dBc
43 MHz	-46 dBc
Low-gain amplifier path	

22. Amplitude -1 dBFS. Includes the 2 through the 6 harmonics.

20 kHz	-77 dBc, typical
1 MHz	-70 dBc, typical
5 MHz	-68 dBc
10 MHz	-61 dBc
20 MHz	-53 dBc
30 MHz	-48 dBc
40 MHz	-46 dBc
43 MHz	-45 dBc
High-gain amplifier path	
20 kHz	-77 dBc, typical
1 MHz	-62 dBc, typical
5 MHz	-55 dBc
10 MHz	-46 dBc
THD[22] (0 °C to 55 °C)	

Direct path	
20 kHz	-76 dBc, typical
1 MHz	-74 dBc, typical
5 MHz	-67 dBc
10 MHz	-63 dBc
20 MHz	-54 dBc
30 MHz	-48 dBc
40 MHz	-45 dBc
43 MHz	-44 dBc
Low-gain amplifier path	
20 kHz	-76 dBc, typical
1 MHz	-69 dBc, typical
5 MHz	-67 dBc
10 MHz	-60 dBc

20 MHz	-52 dBc
30 MHz	-46 dBc
40 MHz	-41 dBc
43 MHz	-41 dBc
High-gain amplifier path	
20 kHz	-76 dBc, typical
1 MHz	-61 dBc, typical
5 MHz	-54 dBc
10 MHz	-45 dBc

Average Noise Density[23]

Direct path	
1 Vpk-pk, 4.0 dBm amplitude range	18 $\frac{nV}{\sqrt{Hz}}$, -142 dBm/Hz, -146.0 dBFS/Hz
Low-gain amplifier path	

23. Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor.

0.06 Vpk-pk, -20.4 dBm amplitude range	9 $\frac{nV}{\sqrt{Hz}}$, -148 dBm/Hz, -127.6 dBFS/Hz
0.1 Vpk-pk, -16.0 dBm amplitude range	9 $\frac{nV}{\sqrt{Hz}}$, -148 dBm/Hz, -132.0 dBFS/Hz
0.4 Vpk-pk, -4.0 dBm amplitude range	13 $\frac{nV}{\sqrt{Hz}}$, -145 dBm/Hz, -141.0 dBFS/Hz
1 Vpk-pk, 4.0 dBm amplitude range	18 $\frac{nV}{\sqrt{Hz}}$, -142 dBm/Hz, -146.0 dBFS/Hz
2 Vpk-pk, 10.0 dBm amplitude range	35 $\frac{nV}{\sqrt{Hz}}$, -136 dBm/Hz, -146.0 dBFS/Hz
High-gain amplifier path	
4 Vpk-pk, 16.0 dBm amplitude range	71 $\frac{nV}{\sqrt{Hz}}$, -130 dBm/Hz, -146.0 dBFS/Hz

12 Vpk-pk, 25.6 dBm amplitude range	213 $\frac{nV}{\sqrt{Hz}}$, -120 dBm/Hz, -145.6 dBFS/Hz

Intermodulation Distortion (IMD)[24]

All values are typical.

Direct path	
10.2 MHz and 11.2 MHz	-81 dBc
10.6 MHz and 10.8 MHz	-81 dBc
19.5 MHz and 20.5 MHz	-78 dBc
19.9 MHz and 20.1 MHz	-78 dBc
34.0 MHz and 35.0 MHz	-75 dBc
34.8 MHz and 35.0 MHz	-75 dBc
42.0 MHz and 43.0 MHz	-75 dBc
42.8 MHz and 43.0 MHz	-75 dBc
Low-gain amplifier path	

24. Each tone is -7 dBFS.

10.2 MHz and 11.2 MHz	-80 dBc
10.6 MHz and 10.8 MHz	-79 dBc
19.5 MHz and 20.5 MHz	-66 dBc
19.9 MHz and 20.1 MHz	-65 dBc
34.0 MHz and 35.0 MHz	-58 dBc
34.8 MHz and 35.0 MHz	-58 dBc
42.0 MHz and 43.0 MHz	-55 dBc
42.8 MHz and 43.0 MHz	-55 dBc
High-gain amplifier path	
10.2 MHz and 11.2 MHz	-62 dBc
10.6 MHz and 10.8 MHz	-61 dBc
19.5 MHz and 20.5 MHz	-54 dBc
19.9 MHz and 20.1 MHz	-50 dBc

34.0 MHz and 35.0 MHz	-51 dBc
34.8 MHz and 35.0 MHz	-51 dBc
42.0 MHz and 43.0 MHz	-51 dBc
42.8 MHz and 43.0 MHz	-50 dBc

Spectrum Performance

The noise floor in the following figures is limited by the measurement device. Refer to Average Noise Density for more information about this limit.

Figure 4. 10 MHz Single-Tone Spectrum, Direct Path, 100 MS/s, Interpolation Factor Set to 4

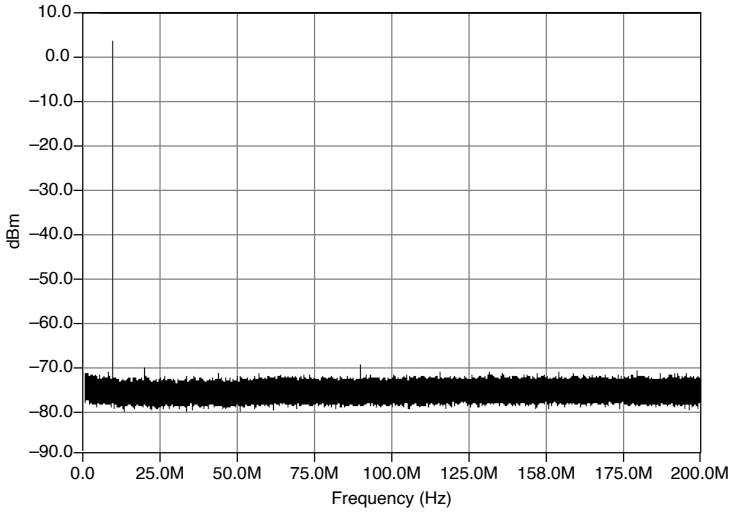


Figure 5. 10 MHz Single-Tone Spectrum, Low-Gain Amplifier Path, 100 MS/s, Interpolation Factor Set

to 4

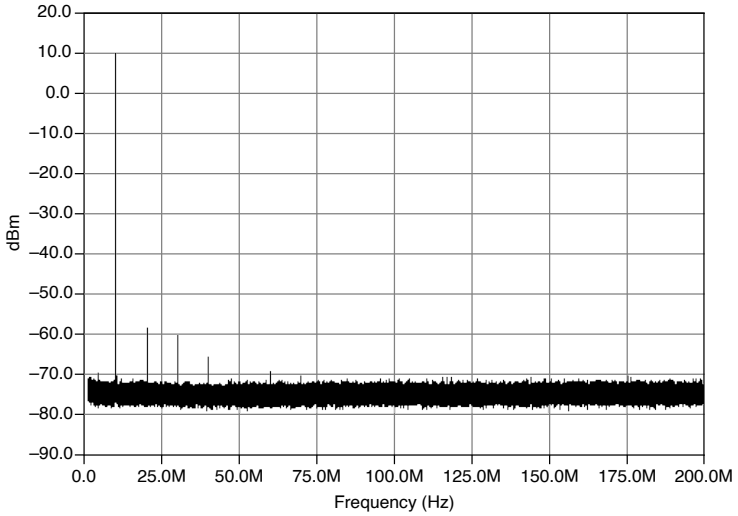
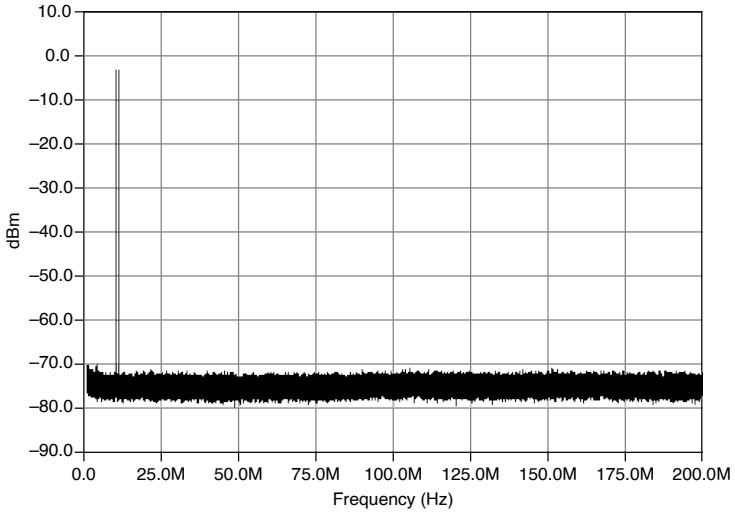


Figure 6. Direct Path, Two-Tone Spectrum, Typical



Sample Clock

Sources	
Internal[25]	Divide-by-N (N ≥ 1) DDS-based, High-Resolution
External	CLK IN (SMB front panel connector) DDC CLK IN (DIGITAL DATA & CONTROL front panel connector)

25. Refer to the Onboard Clock section for more information about internal clock sources.

	External, RTSI<0..7>

Sample Rate Range and Resolution

Sample rate range	
Divide-by-N	23.84 S/s to 100 MS/s
High-Resolution	10 S/s to 100 MS/s
CLK IN	200 kS/s to 105 MS/s
DDC CLK IN	10 S/s to 105 MS/s
RTSI<0..7>	10 S/s to 20 MS/s

Sample rate resolution	
Divide-by-N	Configurable to (100 MS/s) / N (1 ≤ N ≤ 4,194,304)
High-Resolution	1.06 µHz
CLK IN, DDC CLK IN, and RTSI<0..7>	Resolution determined by External Clock source. External Sample Clock duty cycle tolerance 40% to 60%.

Effective Sample Rate

(Interpolation factor) * (Sample rate) = Effective sample rate		
Interpolation factor	**Sample rate**	**Effective sample rate**
1 (Off)	10 S/s to 105 MS/s	10 S/s to 105 MS/s
2	12.5 MS/s to 105 MS/s	25 MS/s to 210 MS/s
4	10 MS/s to 100 MS/s	40 MS/s to 400 MS/s
8	10 MS/s to 50 MS/s	80 MS/s to 400 MS/s

Sample Clock Delay Range and Resolution

Table 9. Delay Adjustment Range

Sample Clock Source	Delay Adjustment Range
Divide-by-N	±1 Sample Clock period
High-Resolution	
CLK IN	0 ns to 7.6 ns
DDC CLK IN	
PXI Star Trigger	
PXI_Trig <0..7>	

Table 10. Delay Adjustment Resolution

Sample Clock Source	Delay Adjustment Resolution
Divide-by-N	<10 ps
High-Resolution	Sample Clock period/16,384
CLK IN	<15 ps
DDC CLK IN	
PXI Star Trigger	

Sample Clock Source	Delay Adjustment Resolution
PXI_Trig <0..7>	

System Phase Noise and Jitter (10 MHz Carrier)

System phase noise density offset[26]	
Divide-by-N	
100 Hz	-110 dBc/Hz
1 kHz	-127 dBc/Hz
10 kHz	-137 dBc/Hz
High-Resolution[27]	
100 Hz	-109 dBc/Hz
1 kHz	-121 dBc/Hz
10 kHz	-123 dBc/Hz
CLK IN	
100 Hz	-113 dBc/Hz
1 kHz	-125 dBc/Hz
10 kHz	-135 dBc/Hz

26. Specified at two times DAC oversampling.

System output jitter (integrated from 100 Hz to 100 kHz)[26]	
Divide-by-N	<2.0 ps rms
High-Resolution[]	<4.2 ps rms
CLK IN	<2.0 ps rms
External Sample Clock input jitter tolerance	
Cycle-cycle jitter	±300 ps
Period jitter	±1 ns

Sample Clock Exporting

Destinations[28][28]	PFI <0..1> (SMB front panel connectors) DDC CLK OUT (DIGITAL DATA & CONTROL front panel connector) RTSI<0..6>
Maximum frequency	
PFI <0..1>	105 MHz
DDC CLK OUT	105 MHz

27. High-Resolution specifications increase as the sample rate is decreased.
28. Exported Sample Clocks can be divided by integer K (1 ≤ K ≤ 4,194,304).

RTSI<0..6>	20 MHz
Jitter	
PFI 0	6 ps rms, typical
PFI 1	12 ps rms, typical
DDC CLK OUT	40 ps rms, typical
Duty cycle	
PFI <0..1>	25% to 65%
DDC CLK OUT	40% to 60%

Onboard Clock (Internal VCXO)

Source	Internal Sample Clocks can either be locked to a Reference Clock using a phase-locked loop or derived from the onboard VCXO frequency reference.
Frequency accuracy	±25 ppm

Phase-Locked Loop (PLL) Reference Clock

Sources[29]	RTSI_7 (RTSI_CLK)

29. The PLL Reference Clock provides the reference frequency for the PLL.

	CLK IN (SMB front panel connector)
Frequency accuracy	When using the PLL, the frequency accuracy of the PCI-5421 is solely dependent on the frequency accuracy of the PLL Reference Clock source.
Lock time	200 ms, maximum 70 ms, typical
Frequency range[30]	5 MHz to 20 MHz in increments of 1 MHz[31]
Duty cycle range	40% to 60%
Destinations	PFI <0..1> (SMB front panel connectors) RTSI<0..6>

CLK IN

Connector type	SMB jack
Direction	Input
Destinations	Sample Clock

30. The PLL Reference Clock frequency must be accurate to ±50 ppm.
31. The default is 10 MHz.

	PLL Reference Clock
Frequency range	
Sample Clock destination and sine waves	1 MHz to 105 MHz
Sample Clock destination and square waves	200 kHz to 105 MHz
PLL Reference Clock destination	5 MHz to 20 MHz
Input voltage range into 50 Ω	
Sine wave	0.65 V pk-pk to 2.8 V pk-pk (0 dBm to +13 dBm)
Square wave	0.2 V pk-pk to 2.8 V pk-pk
Maximum input overload	±10 V
Input impedance	50 Ω
Input coupling	AC

PFI 0 and PFI 1

Connector type	SMB jack (x2)
Direction	Bidirectional

Frequency range	DC to 105 MHz
As an input (trigger)	
Destinations	Start Trigger
Maximum input overload	-2 V to +7 V
V IH	2.0 V
V IL	0.8 V
Input impedance	1 kΩ
As an output (event)	
Sources	Sample Clock divided by integer K (1 ≤ K ≤ 4,194,304) Sample Clock Timebase (200 MHz) divided by integer M (2 ≤ M ≤ 4,194,304) PLL Reference Clock Marker Exported Start Trigger (Out Start Trigger)
Output impedance	50 Ω
Maximum output overload	-2 V to +7 V
Minimum V OH[32]	

Open load	2.9 V
50 Ω load	1.4 V
Maximum V OL[32]	
Open load	0.2 V
50 Ω load	0.2 V
Rise/fall time (20% to 80%)[33]	≤2.0 ns

DIGITAL DATA & CONTROL (DDC)

Connector type	68-pin VHDCI female receptacle
Number of data output signals	16
Control signals	DDC CLK OUT (clock output) DDC CLK IN (clock input) PFI 2 (input) PFI 3 (input) PFI 4 (output)

32. Output drivers are +3.3 V TTL compatible.
33. Load of 10 pF.

	PFI 5 (output)
Ground	23 pins

Output Signals (Data Outputs, DDC CLK OUT, and PFI <4..5>)

Low-voltage differential signal (LVDS)[34]	
V OH	1.3 V, typical 1.7 V, maximum
V OL	0.8 V, minimum 1.0 V, typical
Differential output voltage	0.25 V, minimum 0.45 V, maximum
Output common-mode voltage	1.125 V, minimum 1.375 V, maximum
Rise/fall time (20% to 80%)	0.8 ns, typical 1.6 ns, maximum
Output	1 ns, typical

34. Tested with a 100 Ω differential load, measured at the module front panel, load capacitance <10 pF, driver and receiver comply with ANSI/TIA/EIA-644.

skew[35]	2 ns, maximum
Output enable/ disable	Controlled through the software on all data output signals and control signals collectively. When disabled, the output signals go to a high-impedance state.
Maximum output overload	-0.3 V to +3.9 V

Input Signals (DDC CLK IN and PFI <2..3>)

Signal type	Low-voltage differential signal (LVDS)
Input differential impedance	100 Ω
Maximum output overload	-0.3 V to +3.9 V
Differential input voltage	0.1 V, minimum 0.5 V, maximum
Input common mode voltage	0.2 V, minimum 2.2 V, maximum

35. Skew between any two output signals on the DIGITAL DATA & CONTROL (DDC) front panel connector.

DDC CLK OUT

Clocking format	Data outputs and markers change on the falling edge of DDC CLK OUT.
Frequency range	Refer to the Sample Clock section for more information.
Duty cycle	40% to 60%
Jitter	40 ps rms

DDC CLK IN

Clocking format	DDC data output signals change on the rising edge of DDC CLK IN.
Frequency range	10 Hz to 105 MHz
Input duty cycle tolerance	40% to 60%
Input jitter tolerances	300 ps pk-pk of cycle-cycle jitter 1 ns rms of period jitter

Start Trigger

Sources	PFI<0..1> (SMB front panel connectors) PFI<2..3> (DIGITAL DATA & CONTROL front panel connector)

	RTSI<0..7> Software (use node or function call) Immediate (does not wait for a trigger). The default is Immediate.
Modes	Single Continuous Stepped Burst
Edge detection	Rising
Minimum pulse width	25 ns
Delay from Start Trigger to CH 0 analog output	
Digital interpolation filter disabled	43 Sample Clock periods + 110 ns, typical
Interpolation factor of 2	57 Sample Clock periods + 110 ns, typical
Interpolation factor of 4	63 Sample Clock periods + 110 ns, typical
Interpolation factor of 8	64 Sample Clock periods + 110 ns, typical
Delay from Start Trigger to DDC output	40 Sample Clock periods + 110 ns

Exported trigger destinations	A signal used as a trigger can be routed out to any destination listed in the ***Destinations*** specification of the Markers section
Exported trigger delay	65 ns, typical
Exported trigger pulse width	>150 ns

Markers

Destinations	PFI <0..1> (SMB front panel connectors) PFI <4..5> (DIGITAL DATA & CONTROL front panel connector) RTSI<0..6>
Quantity	One marker per segment
Quantum	Marker position must be placed at an integer multiple of four samples.
Width	>150 ns
Skew with respect to analog output	
PFI <0..1>	±2 Sample Clock periods
PXI_Trig <0..6>	±2 Sample Clock periods
Skew with respect to digital data output	

PFI <4..5>	<2 ns
Jitter	20 ps rms

Arbitrary Waveform Generation Mode

Memory usage	The PCI-5421 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters—such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage—are flexible and user-defined.

Onboard memory size	
8 MB standard	8,388,608 bytes
32 MB option	33,554,432 bytes
256 MB option	268,435,456 bytes
512 MB option	536,870,912 bytes

Output modes	Arbitrary waveform[36] [36] Arbitrary sequence[37] [37]

36. In arbitrary waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.
37. In arbitrary sequence mode, a sequence directs the PCI-5421 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as ***segments***. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which

Table 11. Minimum Waveform Size

Trigger Mode	Minimum Waveform Size (Samples)		
	Arbitrary Waveform Mode	Arbitrary Sequence Mode[38]	
		At >50 MS/s	At ≤50 MS/s
Single	16		
Continuous	16 samples	96 samples at >50 MS/s	32 samples at ≤50 MS/s
Stepped			
Burst			

Loop count	1 to 16,777,215 Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of four samples.

Memory Limits

Note All trigger modes except where noted.

Table 12. Maximum Waveform Memory

Onboard Memory	Maximum Waveform Memory (Samples)	
	Arbitrary Waveform Mode	Arbitrary Sequence Mode[39][39]
8 MB standard	4,194,176	4,194,120
32 MB option	16,777,088	16,777,008
256 MB option	134,217,600	134,217,520
512 MB option	268,435,328	268,435,200

sample in the waveform a marker output signal is sent.

38. The minimum waveform size is sample rate dependent in arbitrary sequence mode.
39. One or two segments in a sequence.

Table 13. Maximum Waveforms in Arbitrary Sequence Mode[39]

Onboard Memory	Maximum Waveforms
8 MB standard	65,000
	Burst trigger: 8,000
32 MB option	262,000
	Burst trigger: 32,000
256 MB option	2,097,000
	Burst trigger: 262,000
512 MB option	4,194,000
	Burst trigger: 524,000

Table 14. Maximum Segments in a Sequence in Arbitrary Sequence Mode[40]

Onboard Memory	Maximum Segments in a Sequence
8 MB standard	104,000
	Burst trigger: 65,000
32 MB option	418,000
	Burst trigger: 262,000
256 MB option	3,354,000
	Burst trigger: 2,090,000
512 MB option	6,708,000
	Burst trigger: 4,180,000

Calibration

Self-calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.

40. Waveform memory is <4,000 samples.

External calibration	External calibration calibrates the VCXO, voltage reference, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.
Calibration interval	Specifications valid within two years of external calibration.
Warm-up time	15 minutes

Power

All values are typical. Overload operation occurs when CH 0 is shorted to ground.

+3.3 VDC	
Typical operation	1.9 A
Overload operation	2.7 A
+5 VDC	
Typical operation	2.0 A
Overload operation	2.2 A
+12 VDC	
Typical operation	0.46 A
Overload operation	0.5 A

-12 VDC	
Typical operation	0.01 A
Overload operation	0.01 A
Total power	
Typical operation	21.9 W
Overload operation	26.0 W

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-25 °C to 85 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Storage shock	50 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Nonoperating random vibration	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Physical

Dimensions	34.1 cm × 2.0 cm × 10.7 cm (13.4 in. × 0.8 in. × 4.2 in.)
Weight	419 g (14.8 oz)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to ***Product Certifications and Declarations***.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory

compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)