ECUTS-16001 Specifications

2025-03-10

Contents

ECUTS-16001 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Typical-95*** specifications describe the performance met by 95% (≈2σ) of models with a 95% confidence.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Warranted*** unless otherwise noted.

Conditions

Refer to ***ni.com/docs*** for detailed specifications on the specific instruments used within the ECUTS-16001.

Note Other product and company names listed are trademarks or trade names of their respective companies.

These specifications apply to all ECUTS-16001 configuration options unless otherwise noted. Specifications are valid for the system and all included instruments under the following conditions unless otherwise noted.

- ECU Test System environmental characteristics are met

- Instrument-level conditions are met

Calibration Conditions

The performance of an externally calibrated instrument is defined in the instrument specifications. Additionally, specifications for externally calibrated instruments are only valid if the conditions defined in the instrument specifications are met.

Related information:

- ni.com/docs

ECUTS-16001 Mass Interconnect Pinouts

The tables in this document show the pin definitions for each slot type on the mass interconnect.

J1 Pinout

	A	B	C	D	Function
1	DIO1#	DIO2#	GND	ATN#	GPIB
2	DIO3#	DIO4#	GND	SRQ#	
3	DIO5#	DIO6#	GND	IFC#	
4	DIO7#	DIO8#	GND	NDAC#	
5	SHIELD	LOGIC GND	GND	NRFD#	
6			GND	DAV#	
7			GND	EOI#	
8				REN#	
9					
10	P0.0	P0.1	P0.2	P0.3	J1_DIO
11	P0.COM	P0.COM	P0.COM	P0.COM	
12	P0.4	P0.5	P0.6	P0.7	
13	P1.0	P1.1	P1.2	P1.3	
14	P1.COM	P1.COM	P1.COM	P1.COM	
15	P1.4	P1.5	P1.6	P1.7	
16	P2.0	P2.1	P2.2	P2.3	
17	P2.COM	P2.COM	P2.COM	P2.COM	
18	P2.4	P2.5	P2.6	P2.7	
19	P3.0	P3.1	P3.2	P3.3	
20	P3.COM	P3.COM	P3.COM	P3.COM	
21	P3.4	P3.5	P3.6	P3.7	
22	P4.0	P4.1	P4.2	P4.3	
23	P4.COM (P4.VCC)	P4.GND	P4.GND	P4.GND	
24	P4.4	P4.5	P4.6	P4.7	
25	P5.0	P5.1	P5.2	P5.3	
26	P5.COM (P5.VCC)	P5.GND	P5.GND	P5.GND	
27	P5.4	P5.5	P5.6	P5.7	
28	P6.0	P6.1	P6.2	P6.3	
29	P6.COM (P6.VCC)	P6.GND	P6.GND	P6.GND	
30	P6.4	P6.5	P6.6	P6.7	
31	P7.0	P7.1	P7.2	P7.3	
32	P7.COM (P7.VCC)	P7.GND	P7.GND	P7.GND	
33	P7.4	P7.5	P7.6	P7.7	
34	P6 +5V	P7 +5V			
35				SHIELD	NET1
36	Reserved	Reserved	RX+	TX+	
37	Reserved	Reserved	RX-	TX-	
38				SHIELD	NET2
39	Reserved	Reserved	RX+	TX+	
40	Reserved	Reserved	RX-	TX-	
41					
42	CHSGND	CHSGND	CHSGND	CHSGND	
43	PPS Interlock [1]	12 V Interlock[1]	24 V Interlock[1]	User Interlock[1]	Interlock
44	PPS Interlock Return [1]	12 V Interlock Return[1]	24 V Interlock Return[1]	User Interlock Return[1]	
45	Port 1 TRX+	Port 2 TRX+	Port 3 TRX+	Port 4 TRX+	Auto Ethernet
46	Port 1 TRX-	Port 2 TRX-	Port 3 TRX-	Port 4 TRX-	
47	Port 5 TRX+	Port 6 TRX+	Port 7 TRX+	Port 8 TRX+	
48	Port 5 TRX-	Port 6 TRX-	Port 7 TRX-	Port 8 TRX-	

[1] Connect the interlock pins through dry contacts to their associated return pin to enable the respective subsystem.

J2 Pinout

A1	LOAD0+		
		B1	SENSE0+
A2	LOAD0-		
		B2	SENSE0-
A3	LOAD1+		
		B3	SENSE1+
A4	LOAD1-		
		B4	SENSE1-
A5	LOAD2+		
		B5	SENSE2+
A6	LOAD2-		
		B6	SENSE2-
A7	LOAD3+		
		B7	SENSE3+
A8	LOAD3-		
		B8	SENSE3-
A9	LOAD4+		
		B9	SENSE4+
A10	LOAD4-		
		B10	SENSE4-
A11	LOAD5+		
		B11	SENSE5+
A12	LOAD5-		
		B12	SENSE5-
A13	LOAD6+		
		B13	SENSE6+
A14	LOAD6-		
		B14	SENSE6-
A15	LOAD7+		
		B15	SENSE7+
A16	LOAD7-		
		B16	SENSE7-

J3-J8 Pinouts

Figure 1. J3-J8 Pinout when Populated with a PXIe-2520

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5	COM0	COM2	COM5	COM7	RELAY
6	CH0	CH2	CH5	CH7	
7	COM1	COM3	COM6	COM8	
8	CH1	CH3	CH6	CH8	
9	COM4	CH4	COM9	CH9	
10	COM10	COM12	COM15	COM17	
11	CH10	CH12	CH15	CH17	
12	COM11	COM13	COM16	COM18	
13	CH11	CH13	CH16	CH18	
14	COM14	CH14	COM19	CH19	
15	COM20	COM22	COM25	COM27	
16	CH20	CH22	CH25	CH27	
17	COM21	COM23	COM26	COM28	
18	CH21	CH23	CH26	CH28	
19	COM24	CH24	COM29	CH29	
20	COM30	COM32	COM35	COM37	
21	CH30	CH32	CH35	CH37	
22	COM31	COM33	COM36	COM38	
23	CH31	CH33	CH36	CH38	
24	COM34	CH34	COM39	CH39	
25	COM40	COM42	COM45	COM47	
26	CH40	CH42	CH45	CH47	
27	COM41	COM43	COM46	COM48	
28	CH41	CH43	CH46	CH48	
29	COM44	CH44	COM49	CH49	
30	COM50	COM52	COM55	COM57	
31	CH50	CH52	CH55	CH57	
32	COM51	COM53	COM56	COM58	
33	CH51	CH53	CH56	CH58	
34	COM54	CH54	COM59	CH59	
35	COM60	COM62	COM65	COM67	
36	CH60	CH62	CH65	CH67	
37	COM61	COM63	COM66	COM68	
38	CH61	CH63	CH66	CH68	
39	COM64	CH64	COM69	CH69	
40	COM70	COM72	COM75	COM77	
41	CH70	CH72	CH75	CH77	
42	COM71	COM73	COM76	COM78	
43	CH71	CH73	CH76	CH78	
44	COM74	CH74	COM79	CH79	
45	AO0+	AO1+	AO2+	AO3+	AO
46	AO0-	AO1-	AO2-	AO3-	
47	AO4+	AO5+	AO6+	AO7+	
48	AO4-	AO5-	AO6-	AO7-	

Figure 2. J3-J8 Pinout when Populated with a PXIe-2527

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5	See PXIe-2527 Topology Figures Below				MUX_1
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25	See PXIe-2527 Topology Figures Below				MUX_2
26					
27					
28					
29					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
40					
41					
42					
43					
44					
45	AO0+	AO1+	AO2+	AO3+	AO
46	AO0-	AO1-	AO2-	AO3-	
47	AO4+	AO5+	AO6+	AO7+	
48	AO4-	AO5-	AO6-	AO7-	

Figure 3. J3-J8 Pinout when Populated with a PXIe-2527 (1-Wire Topology)

MUX_1	MUX_2	A	B	C	D
5	25	CH 0	CH 2	CH 4	CH 6
6	26	CH 32	CH 34	CH 36	CH 38
7	27	CH 1	CH 3	CH 5	CH 7
8	28	CH 33	CH 35	CH 37	CH 39
9	29	CH 8	CH 10	CH 12	CH 14
10	30	CH 40	CH 42	CH 44	CH 46
11	31	CH 9	CH 11	CH 13	CH 15
12	32	CH 41	CH 43	CH 45	CH 47
13	33	COM 0	1WREF0	COM 1	SHIELD
14	34		1WREF1		
15	35	CH 16	CH 18	CH 20	CH 22
16	36	CH 48	CH 50	CH 52	CH 54
17	37	CH 17	CH 19	CH 21	CH 23
18	38	CH 49	CH 51	CH 53	CH 55
19	39	CH 24	CH 26	CH 28	CH 30
20	40	CH 56	CH 58	CH 60	CH 62
21	41	CH 25	CH 27	CH 29	CH 31
22	42	CH 57	CH 59	CH 61	CH 63
23	43				
24	44				

Figure 4. J3-J8 Pinout when Populated with a PXIe-2527 (2-Wire Topology)

MUX_1	MUX_2	A	B	C	D
5	25	CH 0+	CH 2+	CH 4+	CH 6+
6	26	CH 0-	CH 2-	CH 4-	CH 6-
7	27	CH 1+	CH 3+	CH 5+	CH 7+
8	28	CH 1-	CH 3-	CH 5-	CH 7-
9	29	CH 8+	CH 10+	CH 12+	CH 14+
10	30	CH 8-	CH 10-	CH 12-	CH 14-
11	31	CH 9+	CH 11+	CH 13+	CH 15+
12	32	CH 9-	CH 11-	CH 13-	CH 15-
13	33	COM 0+		COM 1+	SHIELD
14	34	COM 0-		COM 1-	
15	35	CH 16+	CH 18+	CH 20+	CH 22+
16	36	CH 16-	CH 18-	CH 20-	CH 22-
17	37	CH 17+	CH 19+	CH 21+	CH 23+
18	38	CH 17-	CH 19-	CH 21-	CH 23-
19	39	CH 24+	CH 26+	CH 28+	CH 30+
20	40	CH 24-	CH 26-	CH 28-	CH 30-
21	41	CH 25+	CH 27+	CH 29+	CH 31+
22	42	CH 25-	CH 27-	CH 29-	CH 31-
23	43				
24	44				

Figure 5. J3-J8 Pinout when Populated with a PXIe-2527 (4-Wire Topology)

MUX_1	MUX_2	A	B	C	D
5	25	CH 0A+	CH 2A+	CH 4A+	CH 6A+
6	26	CH 0A-	CH 2A-	CH 4A-	CH 6A-
7	27	CH 1A+	CH 3A+	CH 5A+	CH 7A+
8	28	CH 1A-	CH 3A-	CH 5A-	CH 7A-
9	29	CH 8A+	CH 10A+	CH 12A+	CH 14A+
10	30	CH 8A-	CH 10A-	CH 12A-	CH 14A-
11	31	CH 9A+	CH 11A+	CH 13A+	CH 15A+
12	32	CH 9A-	CH 11A-	CH 13A-	CH 15A-
13	33	COM 0A+		COM 0B+	SHIELD
14	34	COM 0A-		COM 0B-	
15	35	CH 0B+	CH 2B+	CH 4B+	CH 6B+
16	36	CH 0B-	CH 2B-	CH 4B-	CH 6B-
17	37	CH 1B+	CH 3B+	CH 5B+	CH 7B+
18	38	CH 1B-	CH 3B-	CH 5B-	CH 7B-
19	39	CH 8B+	CH 10B+	CH 12B+	CH 14B+
20	40	CH 8B-	CH 10B-	CH 12B-	CH 14B-
21	41	CH 9B+	CH 11B+	CH 13B+	CH 15B+
22	42	CH 9B-	CH 11B-	CH 13B-	CH 15B-
23	43				
24	44				

Figure 6. J3-J8 Pinout when Populated with a PXIe-2737

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5	C0+	C2+	C4+	C6+	MATRIX[1]
6	C0-	C2-	C4-	C6-	
7	C1+	C3+	C5+	C7+	
8	C1-	C3-	C5-	C7-	
9	R0+	R0-	R1+	R1-	
10	C8+	C10+	C12+	C14+	
11	C8-	C10-	C12-	C14-	
12	C9+	C11+	C13+	C15+	
13	C9-	C11-	C13-	C15-	
14	R2+	R2-	R3+	R3-	
15	C16+	C18+	C20+	C22+	
16	C16-	C18-	C20-	C22-	
17	C17+	C19+	C21+	C23+	
18	C17-	C19-	C21-	C23-	
19	R0+	R0-	R1+	R1-	
20	C24+	C26+	C28+	C30+	
21	C24-	C26-	C28-	C30-	
22	C25+	C27+	C29+	C31+	
23	C25-	C27-	C29-	C31-	
24	R2+	R2-	R3+	R3-	
25	C32+	C34+	C36+	C38+	
26	C32-	C34-	C36-	C38-	
27	C33+	C35+	C37+	C39+	
28	C33-	C35-	C37-	C39-	
29	R0+	R0-	R1+	R1-	
30	C40+	C42+	C44+	C46+	
31	C40-	C42-	C44-	C46-	
32	C41+	C43+	C45+	C47+	
33	C41-	C43-	C45-	C47-	
34	R2+	R2-	R3+	R3-	
35	C48+	C50+	C52+	C54+	
36	C48-	C50-	C52-	C54-	
37	C49+	C51+	C53+	C55+	
38	C49-	C51-	C53-	C55-	
39	R0+	R0-	R1+	R1-	
40	C56+	C58+	C60+	C62+	
41	C56-	C58-	C60-	C62-	
42	C57+	C59+	C61+	C63+	
43	C57-	C59-	C61-	C63-	
44	R2+	R2-	R3+	R3-	
45	AO0+	AO1+	AO2+	AO3+	AO
46	AO0-	AO1-	AO2-	AO3-	
47	AO4+	AO5+	AO6+	AO7+	
48	AO4-	AO5-	AO6-	AO7-	

[1] Matrix rows and columns are duplicated across the mass interconnect pinout as follows: Row 0 is duplicated on A9:B9, A19:B19, A29:B29, and A39:B39. Row 1 is duplicated on C9:D9, C:19:D19, C29:D29, and C39:D39. Row 2 is duplicated on A14:B14, A24:B24, A34:B34, and A44:B44. Row 3 is duplicated on C14:D14, C24:D24, C34:D34, and C44:D44.

Figure 7. J3-J8 Pinout when Populated with a PXIe-2738

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5	C0+	C2+	C4+	C6+	MATRIX[1]
6	C0-	C2-	C4-	C6-	
7	C1+	C3+	C5+	C7+	
8	C1-	C3-	C5-	C7-	
9	R0+	R0-	R1+	R1-	
10	C8+	C10+	C12+	C14+	
11	C8-	C10-	C12-	C14-	
12	C9+	C11+	C13+	C15+	
13	C9-	C11-	C13-	C15-	
14	R2+	R2-	R3+	R3-	
15	C16+	C18+	C20+	C22+	
16	C16-	C18-	C20-	C22-	
17	C17+	C19+	C21+	C23+	
18	C17-	C19-	C21-	C23-	
19	R0+	R0-	R1+	R1-	
20	C24+	C26+	C28+	C30+	
21	C24-	C26-	C28-	C30-	
22	C25+	C27+	C29+	C31+	
23	C25-	C27-	C29-	C31-	
24	R2+	R2-	R3+	R3-	
25	C0+	C2+	C4+	C6+	
26	C0-	C2-	C4-	C6-	
27	C1+	C3+	C5+	C7+	
28	C1-	C3-	C5-	C7-	
29	R4+	R4-	R5+	R5-	
30	C8+	C10+	C12+	C14+	
31	C8-	C10-	C12-	C14-	
32	C9+	C11+	C13+	C15+	
33	C9-	C11-	C13-	C15-	
34	R6+	R6-	R7+	R7-	
35	C16+	C18+	C20+	C22+	
36	C16-	C18-	C20-	C22-	
37	C17+	C19+	C21+	C23+	
38	C17-	C19-	C21-	C23-	
39	R4+	R4-	R5+	R5-	
40	C24+	C26+	C28+	C30+	
41	C24-	C26-	C28-	C30-	
42	C25+	C27+	C29+	C31+	
43	C25-	C27-	C29-	C31-	
44	R6+	R6-	R7+	R7-	
45	AO0+	AO1+	AO2+	AO3+	AO
46	AO0-	AO1-	AO2-	AO3-	
47	AO4+	AO5+	AO6+	AO7+	
48	AO4-	AO5-	AO6-	AO6-	

[1] Matrix rows and columns are duplicated across the mass interconnect pinout as follows: Row 0 is duplicated on A9:B9 and A19:B19. Row 1 is duplicated on C9:D9 and C:19:D19. Row 2 is duplicated on A14:B14 and A24:B24. Row 3 is duplicated on C14:D14 and C24:D24. Row 4 is duplicated on A29:B29 and A39:B39. Row 5 is duplicated on A34:B34 and A44:B44. Row 6 is duplicated on A34:B34 and A44:B44. Row 7 is duplicated on C34:D34 and C44:D44. Columns 0-31 are duplicated from A5 through D23 and A25 through D43.

Figure 8. J3-J8 Pinout when Populated with a PXIe-2739

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5	C0+	C2+	C4+	C6+	MATRIX[1]
6	C0-	C2-	C4-	C6-	
7	C1+	C3+	C5+	C7+	
8	C1-	C3-	C5-	C7-	
9	R0+	R0-	R1+	R1-	
10	C8+	C10+	C12+	C14+	
11	C8-	C10-	C12-	C14-	
12	C9+	C11+	C13+	C15+	
13	C9-	C11-	C13-	C15-	
14	R2+	R2-	R3+	R3-	
15	C0+	C2+	C4+	C6+	
16	C0-	C2-	C4-	C6-	
17	C1+	C3+	C5+	C7+	
18	C1-	C3-	C5-	C7-	
19	R4+	R4-	R5+	R5-	
20	C8+	C10+	C12+	C14+	
21	C8-	C10-	C12-	C14-	
22	C9+	C11+	C13+	C15+	
23	C9-	C11-	C13-	C15-	
24	R6+	R6-	R7+	R7-	
25	C0+	C2+	C4+	C6+	
26	C0-	C2-	C4-	C6-	
27	C1+	C3+	C5+	C7+	
28	C1-	C3-	C5-	C7-	
29	R8+	R8-	R9+	R9-	
30	C8+	C10+	C12+	C14+	
31	C8-	C10-	C12-	C14-	
32	C9+	C11+	C13+	C15+	
33	C9-	C11-	C13-	C15-	
34	R10+	R10-	R11+	R11-	
35	C0+	C2+	C4+	C6+	
36	C0-	C2-	C4-	C6-	
37	C1+	C3+	C5+	C7+	
38	C1-	C3-	C5-	C7-	
39	R12+	R12-	R13+	R13-	
40	C8+	C10+	C12+	C14+	
41	C8-	C10-	C12-	C14-	
42	C9+	C11+	C13+	C15+	
43	C9-	C11-	C13-	C15-	
44	R14+	R14-	R15+	R15-	
45	AO0+	AO1+	AO2+	AO3+	AO
46	AO0-	AO1-	AO2-	AO3-	
47	AO4+	AO5+	AO6+	AO7+	
48	AO4-	AO5-	AO6-	AO7-	

[1] Matrix rows and columns are duplicated across the mass interconnect pinout as follows: Columns 0-15 are duplicated from A5 through D33, A15 through D23, A25 through D33, and A35 through D44.

Figure 9. J3-J8 Pinout when Populated with a SLSC-12251

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5	DUT0		DUT2		FIU_1
6		DUT1		DUT3	
7	DUT4		DUT6		
8		DUT5		DUT7	
9	DUT 8		DUT10		
10		DUT9		DUT11	
11	DUT12		DUT14		
12		DUT13		DUT15	
13					
14	LOAD0		LOAD2		
15		LOAD1		LOAD3	
16	LOAD4		LOAD6		
17		LOAD5		LOAD7	
18	LOAD8		LOAD10		
19		LOAD9		LOAD11	
20	LOAD12		LOAD14		
21		LOAD13		LOAD15	
22					
23	BUS A		BUS B		
24					
25	DUT0		DUT2		FIU_2
26		DUT1		DUT3	
27	DUT4		DUT6		
28		DUT5		DUT7	
29	DUT 8		DUT10		
30		DUT9		DUT11	
31	DUT12		DUT14		
32		DUT13		DUT15	
33					
34	LOAD0		LOAD2		
35		LOAD1		LOAD3	
36	LOAD4		LOAD6		
37		LOAD5		LOAD7	
38	LOAD8		LOAD10		
39		LOAD9		LOAD11	
40	LOAD12		LOAD14		
41		LOAD13		LOAD15	
42					
43	BUS A		BUS B		
44					
45	AO0+	AO1+	AO2+	AO3+	AO
46	AO0-	AO1-	AO2-	AO3-	
47	AO4+	AO5+	AO6+	AO7+	
48	AO4-	AO5-	AO6-	AO7-	

J9, J10, and J16 Pinout

1	Pneumatic	Pneumatic
2	DUT0	FIU
3	DUT1	
4	DUT2	
5	DUT3	
6	DUT4	
7	DUT5	
8	DUT6	
9	DUT7	
10	LOAD0	
11	LOAD1	
12	LOAD2	
13	LOAD3	
14	LOAD4	
15	LOAD5	
16	LOAD6	
17	LOAD7	
18	ABA	
19	ABB	

J12 and J14 Pinout

1	FIU-1 DUT0	33	FIU-2 DUT0	65	FIU-3 DUT0
2	FIU-1 DUT1	34	FIU-2 DUT1	66	FIU-3 DUT1
3	FIU-1 DUT2	35	FIU-2 DUT2	67	FIU-3 DUT2
4	FIU-1 DUT3	36	FIU-2 DUT3	68	FIU-3 DUT3
5	FIU-1 DUT4	37	FIU-2 DUT4	69	FIU-3 DUT4
6	FIU-1 DUT5	38	FIU-2 DUT5	70	FIU-3 DUT5
7	FIU-1 DUT6	39	FIU-2 DUT6	71	FIU-3 DUT6
8	FIU-1 DUT7	40	FIU-2 DUT7	72	FIU-3 DUT7
9	FIU-1 DUT8	41	FIU-2 DUT8	73	FIU-3 DUT8
10	FIU-1 DUT9	42	FIU-2 DUT9	74	FIU-3 DUT9
11	FIU-1 DUT10	43	FIU-2 DUT10	75	FIU-3 DUT10
12	FIU-1 DUT11	44	FIU-2 DUT11	76	FIU-3 DUT11
13	FIU-1 DUT12	45	FIU-2 DUT12	77	FIU-3 DUT12
14	FIU-1 DUT13	46	FIU-2 DUT13	78	FIU-3 DUT13
15	FIU-1 DUT14	47	FIU-2 DUT14	79	FIU-3 DUT14
16	FIU-1 DUT15	48	FIU-2 DUT15	80	FIU-3 DUT15
17	FIU-1 LOAD0	49	FIU-2 LOAD0	81	FIU-3 LOAD0
18	FIU-1 LOAD1	50	FIU-2 LOAD1	82	FIU-3 LOAD1
19	FIU-1 LOAD2	51	FIU-2 LOAD2	83	FIU-3 LOAD2
20	FIU-1 LOAD3	52	FIU-2 LOAD3	84	FIU-3 LOAD3
21	FIU-1 LOAD4	53	FIU-2 LOAD4	85	FIU-3 LOAD4
22	FIU-1 LOAD5	54	FIU-2 LOAD5	86	FIU-3 LOAD5
23	FIU-1 LOAD6	55	FIU-2 LOAD6	87	FIU-3 LOAD6
24	FIU-1 LOAD7	56	FIU-2 LOAD7	88	FIU-3 LOAD7
25	FIU-1 LOAD8	57	FIU-2 LOAD8	89	FIU-3 LOAD8
26	FIU-1 LOAD9	58	FIU-2 LOAD9	90	FIU-3 LOAD9
27	FIU-1 LOAD10	59	FIU-2 LOAD10	91	FIU-3 LOAD10
28	FIU-1 LOAD11	60	FIU-2 LOAD11	92	FIU-3 LOAD11
29	FIU-1 LOAD12	61	FIU-2 LOAD12	93	FIU-3 LOAD12
30	FIU-1 LOAD13	62	FIU-2 LOAD13	94	FIU-3 LOAD13
31	FIU-1 LOAD14	63	FIU-2 LOAD14	95	FIU-3 LOAD14
32	FIU-1 LOAD15	64	FIU-2 LOAD15	96	FIU-3 LOAD15

J18-J21 Pinouts

Figure 10. J18-J21 Default Pinout

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5					
6	GUARD				SMU
7	HI	GUARD	LO	CHSGND	
8	GUARD	GUARD	LO SENSE		
9	HI SENSE				
10					
11	AO0+	AO1+	AO2+	AO3+	AO_1
12	AO0-	AO1-	AO2-	AO3-	
13	AO4+	AO5+	AO6+	AO7+	
14	AO4-	AO5-	AO6-	AO7-	
15					
16	AO0+	AO1+	AO2+	AO3+	AO_2
17	AO0-	AO1-	AO2-	AO3-	
18	AO4+	AO5+	AO6+	AO7+	
19	AO4-	AO5-	AO6-	AO7-	
20					
21	AI0+	AI1+	AI2+	AI3+	AI
22	AI0-	AI1-	AI2-	AI3-	
23	COM0	COM1	COM2	COM3	
24	AI4+	AI5+	AI6+	AI7+	
25	AI4-	AI5-	AI6-	AI7-	
26	COM4	COM5	COM6	COM7	
27			PFI0	PFI1	
28	CHSGND	CHSGND			PPS
29	OUT0+	SENSE0+	OUT1+	SENSE1+	
30	OUT0-	SENSE0-	OUT1-	SENSE1-	
31					
32	AI0+	AI1+	AI2+	AI3+	SMIO
33	AI0-	AI1-	AI2-	AI3-	
34	AIGND0	AIGND1	AIGND2	AIGND3	
35	AI4+	AI5+	AI6+	AI7+	
36	AI4-	AI5-	AI6-	AI7-	
37	AIGND4	AIGND5	AIGND6	AIGND7	
38	RESERVED	APFI0	AO0	AO1	
39	+5V	Shield	AOGND0	AOGND1	
40	P0.0	P0.1	P0.2	P0.3	
41	DGND0	DGND1	DGND2	DGND3	
42	P0.4	P0.5	P0.6	P0.7	
43	P1.0	P1.1	P1.2	P1.3	
44	DGND4	DGND5	DGND6	DGND7	
45	P1.4	P1.5	P1.6	P1.7	
46	P2.0	P2.1	P2.2	P2.3	
47	DGND8	DGND9	DGND10	DGND11	
48	P2.4	P2.5	P2.6	P2.7	

Figure 11. J18-J21 Pinout when Populated with a PXIe-6378

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5					
6	GUARD				SMU
7	HI	GUARD	LO	CHSGND	
8	GUARD	GUARD	LO SENSE		
9	HI SENSE				
10					
11	AO0+	AO1+	AO2+	AO3+	AO_1
12	AO0-	AO1-	AO2-	AO3-	
13	AO4+	AO5+	AO6+	AO7+	
14	AO4-	AO5-	AO6-	AO7-	
15					
16	AO0+	AO1+	AO2+	AO3+	AO_2
17	AO0-	AO1-	AO2-	AO3-	
18	AO4+	AO5+	AO6+	AO7+	
19	AO4-	AO5-	AO6-	AO7-	
20					
21	AI0+	AI1+	AI2+	AI3+	AI
22	AI0-	AI1-	AI2-	AI3-	
23	COM0	COM1	COM2	COM3	
24	AI4+	AI5+	AI6+	AI7+	
25	AI4-	AI5-	AI6-	AI7-	
26	COM4	COM5	COM6	COM7	
27			PFI0	PFI1	
28	CHSGND	CHSGND			PPS
29	OUT0+	SENSE0+	OUT1+	SENSE1+	
30	OUT0-	SENSE0-	OUT1-	SENSE1-	
31				SHIELD	AO (PXIe-6738)
32	AO0	AO1	AO2	AO3	
33	A04	A05	A06	AO7	
34	AOGND0_1	AOGND4_5	AOGND2_3	AOGND6_7	
35	AO8	AO9	AO10	AO11	
36	AO12	AO13	AO14	AO15	
37	AOGND8_9_10	AOGND12_13	AOGND11	AOGND14_15	
38	AO16	AO17	AO18	AO19	
39	+5V	DGND	AOGN16_17	AOGND18_19	
40	AO20	AO21	AO22	AO23	
41	AOGND20_21	AOGND24_25	AOGND22_23	AOGND26_27	
42	AO24	AO25	AO26	AO27	
43	AO28	AO29	AO30	AO31	
44	AOGND28_29	AOGND_A_0	AOGND30_31	AOGND_A_1	
45	DGNDP0.0_P0.1	DGNDP1.0_P1.1	P0.0	P0.1	
46	P1.0	P1.1	P1.2	P1.3	
47	DGNDP1.4_P1.5	DGND	DGNDP1.2_P1.3	DGNDP1.6_P1.7	
48	P1.4	P1.5	P1.6	P1.7	

Figure 12. J18-J21 Pinout when Populated with a PXIe-4309

	A	B	C	D	Function
1	HI		HI SENSE		DMM
2					
3		LO		LO SENSE	
4					
5					
6	GUARD				SMU
7	HI	GUARD	LO	CHSGND	
8	GUARD	GUARD	LO SENSE		
9	HI SENSE				
10					
11	AO0+	AO1+	AO2+	AO3+	AO_1
12	AO0-	AO1-	AO2-	AO3-	
13	AO4+	AO5+	AO6+	AO7+	
14	AO4-	AO5-	AO6-	AO7-	
15					
16	AO0+	AO1+	AO2+	AO3+	AO_2
17	AO0-	AO1-	AO2-	AO3-	
18	AO4+	AO5+	AO6+	AO7+	
19	AO4-	AO5-	AO6-	AO7-	
20					
21	AI0+	AI16+	AI8+	AI24+	AI (PXIe-4309)
22	AI0-	AI16-	AI8-	AI24-	
23	GND	GND	GND	GND	
24	AI4+	AI20+	AI12+	AI28+	
25	AI4-	AI20-	AI12-	AI28-	
26	GND	GND	GND	PFIGND	
27	REF+	REF-	PFI0	PFI1	
28	CHSGND	CHSGND			PPS
29	OUT0+	SENSE0+	OUT1+	SENSE1+	
30	OUT0-	SENSE0-	OUT1-	SENSE1-	
31				SHIELD	AI (PXIe-4309)
32	AI1+	AI17+	AI9+	AI25+	
33	AI1-	AI17-	AI9 -	AI25-	
34	GND	GND	GND	GND	
35	AI5+	AI21+	AI13+	AI29+	
36	AI5-	AI21-	AI13-	AI29-	
37	AI2+	AI18+	AI10+	AI26+	
38	AI2-	AI18-	AI10-	AI26-	
39	N/C	SHIELD	GND	GND	
40	A6+	AI22+	AI14+	AI30+	
41	A6 -	AI22-	AI14-	AI30-	
42	GND	GND	GND	GND	
43	AI3+	AI19+	AI11+	AI27+	
44	AI3-	AI19-	AI11-	AI27-	
45	GND	GND	GND	GND	
46	AI7+	AI23+	AI15+	AI31+	
47	AI7 -	AI23-	AI15-	AI31-	
48	GND	GND	GND	GND	

J22 Pinouts

Figure 13. J22 Pinout when Populated with PXIe-5105 Oscilloscopes

		Function			Function			Function
1	12 V					34	24 V	DC Supplies
			18	CHSGND				
2	12 V COM					35	24 V COM	
			19	CH0				
3	CH0					36	CH0	
			20	CH1				
4	CH1					37	CH1	
			21	CH2				J22_FGEN_1
5	CH2					38	PFI0	
			22	CH3				
6	CH3					39	PFI1	
			23	CH4	J22_SCOPE_2			
7	CH4	J22_SCOPE_1				40	CH0	
			24	CH5				
8	CH5					41	CH1	
			25	CH6				J22_FGEN_2
9	CH6					42	PFI0	
			26	CH7				
10	CH7					43	PFI1	
			27	PFI1				
11	PFI1					44		
			28					
12	ABA					45	ABB	J12-FIU1
			29					
13	ABA					46	ABB	J12-FIU2
			30					
14	ABA					47	ABB	J12-FIU3
			31					
15	ABA					48	ABB	J14-FIU1
			32					
16	ABA					49	ABB	J14-FIU2
			33					
17	ABA					50	ABB	J14-FIU3

Figure 14. J22 Pinout when Populated with PXIe-5110 Oscilloscopes

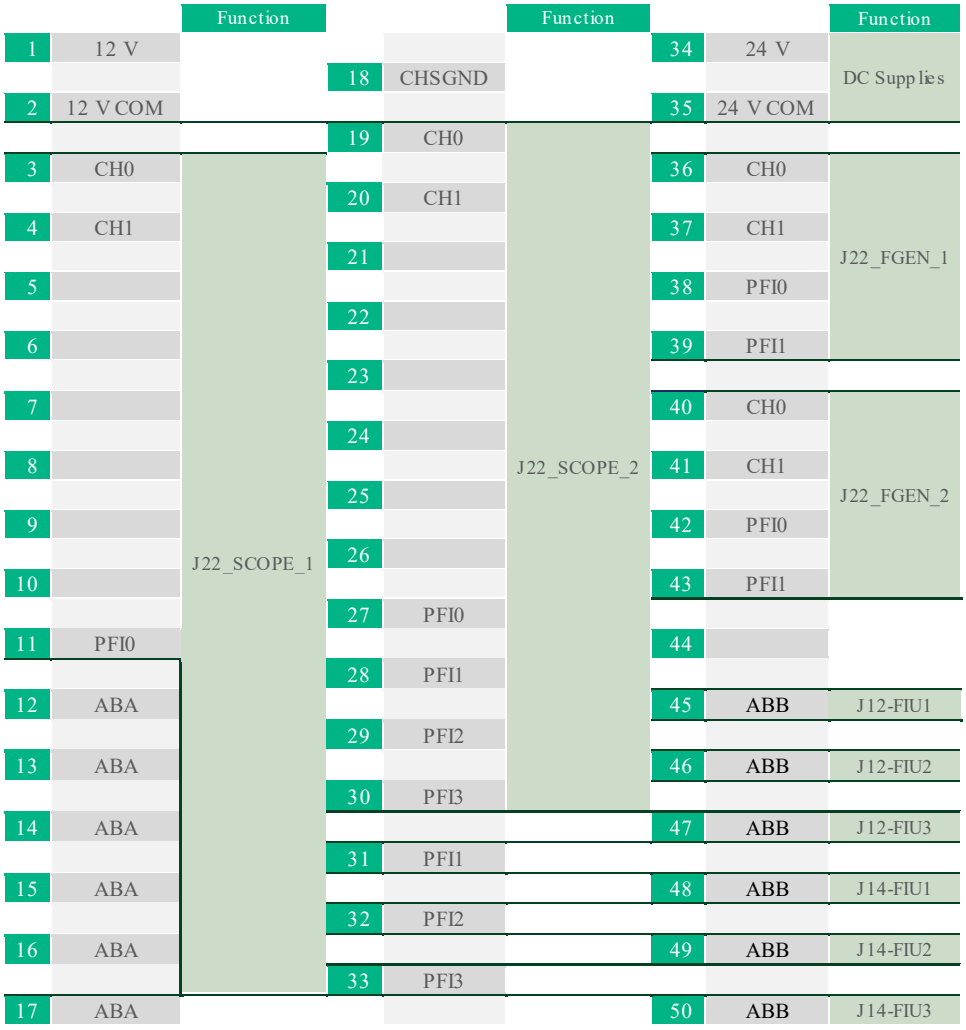

Figure 15. J22 Pinout when Populated with PXIe-5163 Oscilloscopes

		Function			Function			Function
1	12 V					34	24 V	DC Supplies
			18	CHSGND				
2	12 V COM					35	24 V COM	
			19	CH0				
3	CH0					36		
			20	CH1				
4	CH1					37		
			21					
5						38		
			22					
6						39		
			23					
7					J22_SCOPE_2	40		
			24					
8						41		
		J22_SCOPE_1	25					
9						42		
			26					
10						43		
			27	PFI0				
11	PFI0					44		
			28	CLKIN				
12	ABA					45	ABB	J12-FIU1
			29					
13	ABA					46	ABB	J12-FIU2
			30					
14	ABA					47	ABB	J12-FIU3
			31	CLKIN				
15	ABA					48	ABB	J14-FIU1
			32					
16	ABA					49	ABB	J14-FIU2
			33					
17	ABA					50	ABB	J14-FIU3

J23 Pinout

Figure 16. J23 Pinout

	A	B	C	D	Function
1	CAN or LIN Ports 1 and 2				CAN/LIN
2					
3					
4	CAN or LIN Ports 3 and 4				
5					
6					
7	CAN or LIN Ports 5 and 6				
8					
9					
10					
11	CAN or LIN Ports 7 and 8				CAN/LIN
12					
13					
14	CAN or LIN Ports 9 and 10				
15					
16					
17	CANor LIN Ports 11 and 12				
18					
19					
20					
21	COM2 RXD	COM2 DTR	COM3 DTR	COM3 RXD	RS232
22	COM2 RI	COM2 DSR	COM3 DSR	COM3 RI	
23	COM2 DCD	COM2 RTS	COM3 RTS	COM3 DCD	
24	COM2 TXD	COM2 CTS	COM3 CTS	COM3 TXD	
25		GND	GND		
26	COM4 RXD	COM4 DTR	COM5 DTR	COM5 RXD	
27	COM4 RI	COM4 DSR	COM5 DSR	COM5 RI	
28	COM4 DCD	COM4 RTS	COM5 RTS	COM5 DCD	
29	COM4 TXD	COM4 CTS	COM5 CTS	COM5 TXD	
30					
31	COM6 RXD	COM6 DTR	COM7 DTR	COM7 RXD	
32	COM6 RI	COM6 DSR	COM7 DSR	COM7 RI	
33	COM6 DCD	COM6 RTS	COM7 RTS	COM7 DCD	
34	COM6 TXD	COM6 CTS	COM7 CTS	COM7 TXD	
35		GND	GND		
36	COM8 RXD	COM8 DTR	COM9 DTR	COM9 RXD	
37	COM8 RI	COM8 DSR	COM9 DSR	COM9 RI	
38	COM8 DCD	COM8 RTS	COM9 RTS	COM9 DCD	
39	COM8 TXD	COM8 CTS	COM9 CTS	COM9 TXD	
40					
41	CH0	CH1	CH2	CH3	J23_RELAY
42	COM0	COM1	COM2	COM3	
43	CH4	CH5	CH6	CH7	
44	COM4	COM5	COM6	COM7	
45	CH8	CH9	CH10	CH11	
46	COM8	COM9	COM10	COM11	
47	CH12	CH13	CH14	CH15	
48	COM12	COM13	COM14	COM15	

Figure 17. J23 Pinout CAN Port Pair

A	B	C	D
CAN(x) LO	CAN(x) SHIELD	CAN(x+1) SHIELD	CAN(x+1) LO
CAN(x) HI	CAN(x) VSUP	CAN(x+1) VSUP	CAN(x+1) HI
CAN(x) COM	CAN(x) COM	CAN(x+1) COM	CAN(x+1) COM

Figure 18. J23 Pinout LIN Port Pair

A	B	C	D
No connect	LIN(x) SHIELD	LIN(x+1) SHIELD	No connect
LIN(x)	LIN(x) VSUP	LIN(x+1) VSUP	LIN(x+1)
LIN(x) COM	LIN(x) COM	LIN(x+1) COM	LIN(x+1) COM

J24 Pinout

				Function
A1	OUT+			
		B1	SENSE+	J24_PPS_1
A2	OUT-			
		B2	SENSE-	
A3	OUT+			
		B3	SENSE+	J24_PPS_2
A4	OUT-			
		B4	SENSE-	
A5	OUT+			
		B5	SENSE+	J24_PPS_3
A6	OUT-			
		B6	SENSE-	
A7	OUT+			
		B7	SENSE+	J24_PPS_4
A8	OUT-			
		B8	SENSE-	
A9	OUT+			
		B9	SENSE+	J24_PPS_5
A10	OUT-			
		B10	SENSE-	
A11	OUT+			
		B11	SENSE+	J24_PPS_6
A12	OUT-			
		B12	SENSE-	
A13	OUT+			
		B13	SENSE+	J24_PPS_7
A14	OUT-			
		B14	SENSE-	
A15	OUT+			
		B15	SENSE+	J24_PPS_8
A16	OUT-			
		B16	SENSE-	

Physical Characteristics

Dimensions	
Width, all configurations	584 mm (23.0 in.)
Depth	
Without 9025TR platform[1]	884 mm (34.8 in.)

1. Depth of the system without the 9025TR platform assumes a folded open keyboard tray.

With 9025TR platform	1,356 mm (53.4 in.)
Height, all configurations	2,068 mm (84.1 in.)
Total system weight[2]	
Minimum	267 kg (589 lb)
Maximum	453 kg (1,000 lb)
Maximum fixture weight	
9025TR platform	18 kg at 510 mm (40 lb at 20 in.)
Fixture[3]	18 kg at 510 mm (40 lb at 20 in.)
Keyboard tray	0.9 kg (2 lb)
Human-Machine interface weight	
Keyboard tray	0.9 kg (2 lb)
Monitor	3.5 kg (8 lb)
Rack paint	
Color	RAL-7035 gray

2. The weight of the system depends on which options are purchased and installed.
3. Maximum weight limit when a fixture is attached to the ECUTS-16001 without the 9025TR platform.

Paint type	ESD dissipative paint as defined in IEC 61340-5-1

The circuit breaker on the power entry panel PEP-130 is rated for a mechanical impact energy level of IK06 (1 J), when tested with a direct vertical impact per IEC 61010-1, 3rd Ed., Table 15 and Clause 8.2. The circuit breaker should be guarded against impacts exceeding 1 J.

Protective Earthing

High levels of leakage current may be present on the ECUTS-16001. Connect the ECUTS-16001 protective earth terminal before connecting to AC power.

Note The facility installation shall provide a means for connection to protective earth, and qualified personnel shall install a protective earthing conductor from the ECUTS-16001 protective earthing terminal to the protective earth wire in the facility.

Protective earth terminal wiring	
Grounding wire	2.1 mm^2 (14 AWG)
Ring lug	
Size	M8
Length	20 mm (0.8 in.)
Minimum protective earth terminal torque	1.29 N · m (11.5 lb · in.)

Power Requirements

Note The AC power cords used in the ECUTS-16001 are specially designed for the ECUTS-16001. Do not use these power cords in other electrical appliances. Contact your assigned NI Hardware Services Project Manager for system-specific power cords and associated part numbers.

Note All equipment inside the rack must be powered, directly or indirectly, through the power entry panel PEP-130. Other sources of external power must not be used.

Input voltage range	200 V AC to 240 V AC, 50/60 Hz, single phase, 24 A, maximum
Input power receptacle	IEC 60309 2P+E 6H 32 A
Ring lug	
Size	M8
Length	21 mm (0.8 in.)

The ECUTS-16001 shipment contains a power cord that corresponds to your country of operation.

Maximum Thermal Load

Minimum rating for internal equipment	50 °C
Maximum allowable internal dissipation	

40 °C ambient	1,350 W
28 °C ambient	3,400 W
23 °C ambient	4,300 W

Compressed Air

Air type	Clean, dry air
Connector type	6 mm outer diameter
Maximum pressure	100 PSI (690 kPa)

DC Output

Note Refer to the ***ECUTS-16001 User Manual*** for more information about connector and pin locations.

Table 1. DC Output

PDU	Nominal Voltage	Rated Output Current	Overcurrent Protection	Location and Use	Interlock
DC1	12 V	4 A	20 A	Connector J22, pin 1 referenced to pin 2, fixture power	Connector J1, short, dry contact between pins B43 and B44

PDU	Nominal Voltage	Rated Output Current	Overcurrent Protection	Location and Use	Interlock
DC2	24 V	2 A	10 A	Connector J22, pin 34 referenced to pin 35, fixture power	Connector J1, short, dry contact between connectors C43 and C44
DC3[4]	24 V	5 A	10 A	Internal, fans and instrumentation	—
DC4	48 V	2 A	5 A	Internal, network switch	—

RMX-410x (optional)	
Interlock	Connector J1, short, dry contact between pins A43 and A44
Maximum total output power	2,000 W
N67xx (optional)	
Interlock	Connector J1, short, dry contact between pins D43 and D44
Maximum total output power	1,600 W

I/O

Network ports

4. Reserved for NI internal use only.

External	
Type	I219
Standard	IEEE 802.3 Ethernet, 10BASE-T, 100BASE-TX, 1000BASE-T
Speed	10 Mbps, 100 Mbps, 1,000 Mbps
Internal	
Speed	10 Mbps, 100 Mbps
Subnet	169.254.160.xxx
Number of ports	15 switched ports (two for the mass interconnect, up to 13 for instrumentation)
USB ports	
Rear	
Number of ports	2
Type	USB 3.0
Internal (optional)	
Number of ports	7
Type	USB 2.0

Mass Interconnect model	Virginia Panel Corporation 9025/9025TR

Environmental Characteristics

Note This product is intended for use in indoor applications only.

Temperature	
Operating	5 °C to 40 °C
Storage	0 °C to 60 °C
Humidity	
Operating	20% to 80%, noncondensing
Storage	10% to 80%, noncondensing
Pollution degree	2
Maximum altitude	2,000 m
Ventilation clearances	
Top	760 mm (30 in.)
Front and back	300 mm (12 in.)

Hardware Components

The following components are used within the ECUTS-16001.

Note Detailed specifications for hardware components are available online at ***ni.com/docs***.

Table 2. Required Hardware Components

Model		Description
PXI Chassis	PXIe-1084 [5]	18-Slot PXI Chassis
	PXIe-1095	18-Slot High Performance PXI Chassis
PXI Controller	PXIe-8861	2.8 GHz Quad-Core Intel Xeon PXI Controller
	PXIe-8881	3 GHz 18-Core Intel Xeon PXI Controller
RMX-10011		Mid Power 40U Rack with Low Speed Fan Panel
RMX-10050		Single Phase PDU Single Phase PDU with DC Output

Table 3. PXI Instruments

Model	Description	Overriding Ratings in ECUTS[6]	
		Maximum Working Voltage	Maximum Transient Voltage
PXI-2520	80-Channel, 2 A, SPST Relay Module	100 V, CAT I	500 V
PXI-2564	16-Channel, 5 A, SPST Relay Module	100 V, CAT I	500 V
PXI-2527	32-Channel, 2-Wire Multiplexer	60 V	60 V
PXI-2567 [7]	64-Channel Relay Driver Module	—	—

5. An optional secondary PXIe-1084 chassis can be added using a PXIe-8301Thunderbolt™ 3 PXI Remote Control Module.
6. In some cases, integrating a device in an ECUTS imposes a new specification. This table lists device ratings that change in ECUTS.
7. The maximum total drive current per module in the ECUTS-16000 is 10 A.

Model	Description	Overriding Ratings in ECUTS	
		Maximum Working Voltage	Maximum Transient Voltage
PXI-8517	2-Port FlexRay Interface Module	—	—
PXIe-2532B	512-Crosspoint Matrix Switch Module	100 V, CAT I	500 V
PXIe-2737	4 x 64, 2-Wire Matrix Switch Module	100 V, CAT I	500 V
PXIe-2738	8 x 32, 2-Wire Matrix Switch Module	100 V, CAT I	500 V
PXIe-2739	16 x 16, 2-Wire Matrix Switch Module	100 V, CAT I	500 V
PXIe-4081 [8]	7½-Digit Multimeter with 1.8 MS/s Isolated Digitizer	100 V, CAT I (slots J3-J8) 60 V (slots J18-J21)	500 V (slots J3-J8) 60 V (slots J18-J21)
PXIe-4082	6½-Digit Multimeter with 1.8 MS/s Isolated Digitizer, L and C Measurement Support	100 V, CAT I (slots J3-J8) 60 V (slots J18-J21)	500 V (slots J3-J8) 60 V (slots J18-J21)
PXIe-4112	2-Channel, 60 V, 1 A Programmable Power Supply	60 V	60 V
PXIe-4139 (40 W)	±60 V, ±3 A DC, ±10 A Pulsed, 40 W DC, 100 fA precision source measure unit	—	—
PXIe-4139 (20 W)	±60 V, ±3 A DC, ±10 A Pulsed, 20 W DC, 100 fA precision source measure unit	—	—
PXIe-4309	2 MS/s, 28-bit Flexible Resolution Analog Input	—	—
PXIe-4310 with TB-4310 (600V)	8-Channel, 400 kS/s, 16-Bit Isolated Analog Input Module	60 V	60 V
PXIe-4322	8-Channel, 250 kS/s, 16-Bit Isolated Analog Output Module	Isolation and DC	Isolation: 500 V (slots

8. Add ±15 µV to the DC accuracy specifications in the *PXIe-4081* ***Specifications*** on ***ni.com/docs*** when used in the ECUTS. Do not add this value to the performance limits specified in a calibration procedure or calibration certificate for the PXIe-4081.

Model	Description	Overriding Ratings in ECUTS	
		Maximum Working Voltage	Maximum Transient Voltage
		Overvoltage: 100 V, CAT I (slots J3-J8) 60 V (slots J18-J21)	J3-J8) 60 V (slots J18-J21)
PXIe-5105	8-Channel, 60 MHz Bandwidth, 12-Bit Oscilloscope	—	—
PXIe-5110	2-Channel, 100 MHz Bandwidth, 8-bit Oscilloscope	100 V, CAT I	250 V
PXIe-5163	2-Channel, 200 MHz Bandwidth, 14-bit Oscilloscope	100 V, CAT I	250 V
PXIe-5413	2-Channel, 20 MHz Bandwidth, 16-Bit Waveform Generator	—	—
PXIe-5433	2-Channel, 80 MHz Bandwidth, 16-bit Waveform Generator	—	—
PXIe-6366	8 AI (16-bit, 2 MS/s/ch), 2 AO, 24 DIO Multifunction I/O Module	—	—
PXIe-6386	8 AI (16-Bit, 14 MS/s/ch), 2 AO, 24 DIO Multifunction I/O Module	—	—
PXI-6515	64-Channel, ±30 VDC, 32 Sink/Source Inputs, 32 Sink Outputs, Bank-Isolated Digital I/O Module	—	—
PXIe-6738	16-bit, 32-Channel, 1 MS/s PXI Analog Output Module	—	—
PXIe-8430/8	8-Port, RS232 Serial Interface Module	—	—
PXIe-8510 with TRC-8543 and/or TRC-8546 Transceiver Cable	6-Port Vehicle Multiprotocol Interface Module with CAN or LIN Transceivers	—	—
PXIe-8523	PXIe, 4-Port, 100/1000BASE-T1[9] PXI	—	—

Model	Description	Overriding Ratings in ECUTS	
		Maximum Working Voltage	Maximum Transient Voltage
	Automotive Ethernet Interface Module		

Table 4. Load Switching

Model	Description	Overriding Ratings in ECUTS[10]	
		Maximum Working Voltage	Maximum Transient Voltage
SLSC-12001	12-Slot Chassis for SLSC	—	—
SLSC-12251 [11]	16-Channel, 8 A Fault Insertion Module	100 V, CAT I	500 V
SLSC-12252 [12]	8-Channel, 30 A Fault Insertion Module	100 V, CAT I	500 V
PXIe-6375	PXIe, 208 AI (16-Bit, 3.8 MS/s), 2 AO, 24 DIO, PXI Multifunction I/O Module	—	—

Table 5. Power Supplies and Electronic Loads

Model	Description
RMX-4101	20 V, 10 A, Programmable Power Supply Device
	36 V, 6 A, Programmable Power Supply Device
	60 V, 3.5 A, Programmable Power Supply Device
RMX-4102	20 V, 20 A, Programmable Power Supply Device

9. The PXIe-8523 is limited to 100 Mbit when operating the channels in parallel or up to 1000 Mbit on a single channel.
10. In some cases, integrating a device in an ECUTS imposes a new specification. This table lists device ratings that change in ECUTS.
11. Limit maximum current to 5 A per channel for SLSC-12251 modules routed to the J3-J8 QuadraPaddle slots.
12. The maximum allowable current in an SLSC-12252 channel is 30 A.

Model	Description
	36 V, 12 A, Programmable Power Supply Device
	60 V, 7 A, Programmable Power Supply Device
RMX-4104	20 V, 40 A Programmable Power Supply Device
	36 V, 24 A Programmable Power Supply Device
	60 V, 14 A Programmable Power Supply Device
N6752A/761	50 V, 10 A, 100 W Supply, with Output Disconnect
N6753A/761	20 V, 50 A, 300 W Supply, with Output Disconnect
N6754A/761	60 V, 20 A, 300 W Supply, with Output Disconnect
N6762A/761	Precision 50 V, 3 A, 100 W Supply, with Output Disconnect
N6763A/761	Precision 20 V, 50 A, 300 W Supply, with Output Disconnect
N6764A/761	Precision 60 V, 20 A, 300 W Supply, with Output Disconnect
N6700C	4-Slot 400 W Power System Mainframe
N6791A	60 V, 20 A, 100 W Electronic Load
N6792A	60 V, 40 A, 200 W Electronic Load

Table 6. High-Voltage Cables and Assemblies

Part Number	Description	Maximum Working Voltage	Maximum Transient Voltage
132503-03	ECUTS B3-3 PXIe-4322 Cable	100 V pk	500 V pk
132504-01	ECUTS B4-1 Switch Cable	100 V pk	500 V pk
132504-02	ECUTS B4-2 Switch, DMM, and PXIe-4322 Cable	100 V pk	500 V pk
132504-04	ECUTS B4-4 SLSC-12251, DMM, and PXIe-4322 Cable	100 V pk	500 V pk

Part Number	Description	Maximum Working Voltage	Maximum Transient Voltage
132504-05	ECUTS B4-5 PXIe-2527 and DMM Cable	100 V pk	500 V pk
132504-06	ECUTS, B4-6, VPC Quadrapaddle Signal to DMM and 2x 78 Pin Female DSUB	100 V pk	500 V pk
136249-01	ECUTS B4-7 PXIe-2532B and DMM Interface Assembly	100 V pk	500 V pk
132505-0x	ECUTS B5-x SLSC-12251 Cable	100 V pk	500 V pk
132506-01	ECUTS B6 SLSC-12252 Cable	100 V pk	500 V pk
132508-05	ECUTS B8-5 Multifunction Cable	100 V pk	500 V pk
132508-06	ECUTS B8-6 Multifunction Cable	100 V pk	500 V pk
132508-07	ECUTS B8-7 Multifunction Cable	100 V pk	500 V pk
132508-08	ECUTS B8-8 Multifunction Cable	100 V pk	500 V pk
132509-0x	ECUTS B9-x RMX-400x Cable	80 V pk	80 V pk

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