# SPECIFICATIONS NI Digital Systems Development Board

The NI Digital Systems Development Board (DSDB) was designed for educators to teach digital electronics. The board was designed around the Xilinx Zynq®-7000 family all programmable system-on-chip (SoC) architect. This ensures there is plenty of power for students to learn a wide range of topics ranging from simple combination logic to advanced digital systems and control.

## NI Digital System Development Board

- Digital electronics teaching platform
- Programmable with Multisim, LabVIEW, and Vivado
- Integrates with NI ELVIS II/II+
- Zynq XC7Z020 FPGA
- 8 LEDs, 8 slide switches, 4 push buttons
- Expansion connector
- Capacitive touchscreen
- 3 PMOD connectors





### Peripherals

The DSDB is populated with peripherals found in many products that students can learn to interface with through hands-on experiments. The DSDB contains the following peripherals:

- Audio codec in and out jacks
- Headphone and microphone jacks
- VGA connector
- HDMI
- Ethernet RJ-45 connector
- MicroSD port
- 3 PMOD connectors
- 8 LEDs
- 8 slide switches
- 4 push buttons
- Capacitive touchscreen
- OLED 12 × 32 monochrome display
- 4-digits 7-segments LEDs
- MXP expansion connector
- USB HID
- Breadboard

### **NI ELVIS Integrations**

The NI Educational Laboratory Virtual Instrumentation Suite II and II+ (NI ELVIS II Series) is a flexible teaching platform designed for hands-on experiments. By connecting different boards to the workstation, educators can teach a wide range of topics such as analog, digital, control, mechatronics, telecommunications and embedded theory. NI ELVIS II series has the following 18 instruments, which are accessed by connecting the DSDB to the NI ELVIS II series workstation. Students can use these instruments, which are configurable in LabVIEW, to perform an array of measurement and signal generation applications.

- 2-channel oscilloscope
- 8-channel oscilloscope
- Bode plotter
- Digital multi-meter (DMM)
- Function generator
- Arbitrary waveform generator
- Octave analyzer
- Digital reader
- Digital writer
- Dynamic signal analyzer

- Digital waveform viewer
- Variable supply
- Audio Equalizer
- Impedance analyzer
- DC level
- Data logger
- 2-Wire current-voltage analyzer
- 3-Wire current-voltage analyzer

## Zynq Features

The on-board Zynq-7Z020 is based on the Xilinx programmable system-on-chip (SoC) architecture. It contains a processing system (PS) consisting of a dual-core ARM<sup>®</sup> Cortex<sup>™</sup> A9 and a programmable logic (PL) section. By integrating a PS and PL into one single device, you add system intelligence to the PS and at the same time have real-time data processing decisions made by the PL. The powerful Zynq chip is loaded with features, making it ideal for learning.



#### Programming the FPGA

You can program the DSDB using VHDL or Verilog language through the Vivado environment. The Vivado HL WebPACK software is free for students—the license and software installation are available from www.xilinx.com.

You can also program the DSDB using LabVIEW FPGA, which is a graphical programming language based on a data flow paradigm. Students with no prior VHDL or Verilog knowledge can quickly develop applications by dragging-and-dropping IOs and connecting them to pre-built functions. From the LabVIEW environment, students can compile and program directly to the DSDB. Visit ni.com/labview for more information.

Another option for programming the DSDB is to use Multisim, which is circuit simulation and schematic capture software. It has a Programmable Logic Device (PLD) schematic for students to build digital circuits using basic gates such as AND, OR and flip-flops. Students can experiment and simulate different configurations before deploying the circuit to the FPGA from the Multisim environment. Visit ni.com/multisim for more information.

## Software Requirements

The software you need to install will depend on which environment you will use to program the DSDB.

- Multisim 14.0.1 or later
- LabVIEW 2015
- LabVIEW FPGA Module 2015
- LabVIEW FPGA Xilinx Tools Vivado 2014.4
  or

Vivado HL WebPACK 2014.x or later tier

DSDB driver

## MXP Expansion Connector

The MXP connector expands the DSDB teaching options by providing connectivity to other products such as the Digilent Motor Adapter, or Quanser teaching products such as the AERO. The MXP connector provides analog in and out, digital IOs, and PWM signals. It supports UART and SPI protocol.



## Order Information

For complete product specifications, pricing and other accessory information, call 800 813 3693 (US) or go to ni.com/ni-elvis.

## Specifications

For complete specifications, see the DSDB reference manual at ni.com/manuals.

### FPGA

FPGA	Zynq XC7Z020-CLG484
Cortex-A9 processor	650 MHz
Low speed peripherals	SPI, UART, CAN, I2C
High speed peripherals	1 G Ethernet, SDIO
Program	JTAG, Quad-SPI Flash, MicroSD
Logic slices	13,300 (6-input LUTs, 8 flip-flop)
Fast block RAM	560 KB
DDR 3	512 MB, 32 bit @1050 MHz

### **Power Requirements**

NI ELVIS II/II+	5 V
Barrel jack	4.6 V to 5.4 V, minimum 2 A
Digital IOs	3.3 V

### **Clock Sources**

FPGA oscillator	50 MHz
Reference clock	125 MHz

#### General

Ethernet	10/100/1000 full duplex
Quad SPI Flash	128 Mb, max. 94 MHz
Micro SD card	50 MHz, class 4 or better
Slide switches	8
Push buttons	4
LEDs indicators	8

7-segment display	4-digit, common cathode
Capacitive touchscreen	5 inches, $800 \times 400$ pixel
OLED display	128 by 32 matrix, 50 MHz SCLK
3.3V breadboard DIO	8
3 8-bit DIO PMOD	2 connect to PL, 1 to PS
VGA connector	16-bit color depth
HDMI	Input or output capabilities
Mic, headphone, line in, line out	
audio codec,48 KHz sampling	USB type A HID
For keyboard and mice	Mini USB
For UART or JTAG	Push button for IC master reset, sub-system reset, PL reset

#### **MXP** Connector

Output voltage	3.3 V
16 DIO	3.3 V, 5 V input compatible
4 analog input	12-bit ADC resolution, 0 V to 5 V
2 analog output	12-bit DAC resolution, 0 V to 5 V
PWM	3
Protocol	SPI, UART

#### NI ELVIS

3 analog input	$\pm 10$ V, 1.0 MS/s, 1.2 MHz bandwidth
2 analog output	±10 V, Update rates 2.8 MS/s, 12-bit DAC resolution
Overvoltage protection AISENSE	15 V off, 25 V on
Dimensions	8.5 in. × 8.5 in.

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