PXIe-5774 Specifications

2025-03-10

Contents

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Typical*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C
- Installed in chassis with slot cooling capacity ≥58 W

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 μA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[1]

Voltage Family (V)	V_{IL} (V)	V_{IH} (V)	V_{OL}(100 µA Load) (V)	V_{OH}(100 µA Load) (V)	Maximum DC Drive Strength (mA)
3.3	0.8	2.0	0.2	3.0	24
2.5	0.7	1.6	0.2	2.2	18
1.8	0.62	1.29	0.2	1.5	16
1.5	0.51	1.07	0.2	1.2	12
1.2	0.42	0.87	0.2	0.9	6

Digital I/O High-Speed Serial MGT

Note For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Data rate	500 Mb/s to 16.375 Gb/s, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O AC coupling capacitor	100 nF

MGT TX± Channels

Minimum differential output voltage[2]	170 mV peak-to-peak into 100 Ω, nominal

1. Voltage levels are guaranteed by design through the digital buffer specifications.
2. 800 mV peak-to-peak when transmitter output swing is set to the maximum setting.

I/O coupling	AC-coupled, includes 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV peak-to-peak to 2000 mV peak-to-peak, nominal
> 6.6 Gb/s	150 mV peak-to-peak to 1250 mV peak-to-peak, nominal

Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor

Reconfigurable FPGA

PXIe-5774 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PXIe-5774 FPGA options.

Table 3. Reconfigurable FPGA Options

	KU040	**KU060**
LUTs	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,920	2,760
Embedded Block RAM	21.1 Mb	38.0 Mb
Data Clock Domain	200 MHz, 16 samples per cycle per channel (dual channel mode), 32 samples per cycle (single channel mode)	
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)	
Data transfers	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA channels	59	

Note The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Analog Input

General Characteristics

Number of channels	2, single-ended, simultaneously sampled
Connector type	SMA

Input impedance	50 Ω, nominal
Input coupling	DC
Sample Clock	
Internal Sample Clock[3][3]	3.2 GHz
External Sample Clock[3]	3.2 GHz
Sample Rate	
Dual channel mode	3.2 GS/s per channel
Single channel mode	6.4 GS/s

Analog-to-digital converter (ADC)	ADC12DJ3200, 12-bit resolution

Typical Specifications

Full-scale input ranges	200 mV peak-to-peak 1 V peak-to-peak
Gain accuracy	
200 mV range	±1.47%

3. In single channel mode the ADC cores are interleaved for an aggregate sample rate of 6.4 GS/s.

1 V range	±1.44%
DC offset	
200 mV range	±0.628 mV
1 V range	±1.269 mV

Vertical offset range	±0.5 full-scale, nominal

Bandwidth (-3 dB)[4]	
-01 variant	200 mV range: 3.00 GHz 1 V range: 2.85 GHz
-02 variant	200 mV range: 1.63 GHz 1 V range: 1.62 GHz

Table 4. Single-Tone Spectral Performance, Dual Channel Mode, 1 V range, -01 Variant

	Input Frequency			
	99.9 MHz	**399 MHz**	**999 MHz**	**1.999 GHz**
SNR* (dBFS)	54.7	54.4	53.9	52.8
SINAD* (dBFS)	54.4	53.8	53.3	52.4
SFDR (dBc)	-65.2	-61.1	-60.3	-63.2
ENOB† (bits)	8.7	8.6	8.5	8.4

4. Normalized to 10 MHz.

	Input Frequency			
	99.9 MHz	399 MHz	999 MHz	1.999 GHz

* Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.

† Calculated from SINAD and corrected to full scale.

Table 5. Single-Tone Spectral Performance, Single Channel Mode, 1 V range, -01 Variant

	Input Frequency			
	99.9 MHz	399 MHz	999 MHz	1.999 GHz
SNR* (dBFS)	54.0	53.9	52.8	50.1
SINAD* (dBFS)	53.9	53.4	52.2	50.0
SFDR (dBc)	-61.3	-60.9	-58.4	-52.3
ENOB† (bits)	8.7	8.6	8.4	8.0

Note: Measured using channel AI0. Spectral performance may be degraded using channel AI1.

* Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.

† Calculated from SINAD and corrected to full scale.

Table 6. Single-Tone Spectral Performance, Dual Channel Mode, 200 mV range, -01 Variant

	Input Frequency			
	99.9 MHz	399 MHz	999 MHz	1.999 GHz
SNR* (dBFS)	52.0	52.0	51.7	50.9
SINAD* (dBFS)	51.9	51.8	51.4	50.7
SFDR (dBc)	-65.1	-61.7	-62	-64.4
ENOB† (bits)	8.3	8.3	8.2	8.1

	Input Frequency			
	99.9 MHz	399 MHz	999 MHz	1.999 GHz

* Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.

† Calculated from SINAD and corrected to full scale.

Table 7. Single-Tone Spectral Performance, Single Channel Mode, 200 mV range, -01 Variant

	Input Frequency			
	99.9 MHz	399 MHz	999 MHz	1.999 GHz
SNR* (dBFS)	51.0	51.0	50.4	48.9
SINAD* (dBFS)	51.0	50.8	50.2	48.9
SFDR (dBc)	-57.8	-58.8	-58.4	-53.3
ENOB† (bits)	8.2	8.1	8.0	7.8

Note: Measured using channel AI0. Spectral performance may be degraded using channel AI1.

* Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.

† Calculated from SINAD and corrected to full scale.

Table 8. Noise Spectral Density, 1 V Range, -01 Variant

Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual channel	15.3	-143.3	-147.3
Single channel	10.2	-146.8	-150.8

Note: Excludes fixed interleaving spurs.

Table 9. Noise Spectral Density, 200 mV Range, -01 Variant

Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual channel	4.3	-154.3	-144.3
Single channel	3.1	-157.1	-147.1
Note: Excludes fixed interleaving spurs.			

Note Noise spectral density is verified using a 50 Ω terminator connected to AI0. Noise Spectral density may be degraded using channel AI1.

Figure 1. Single Tone Spectrum (Dual Channel Mode, 99MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01 Variant), Measured

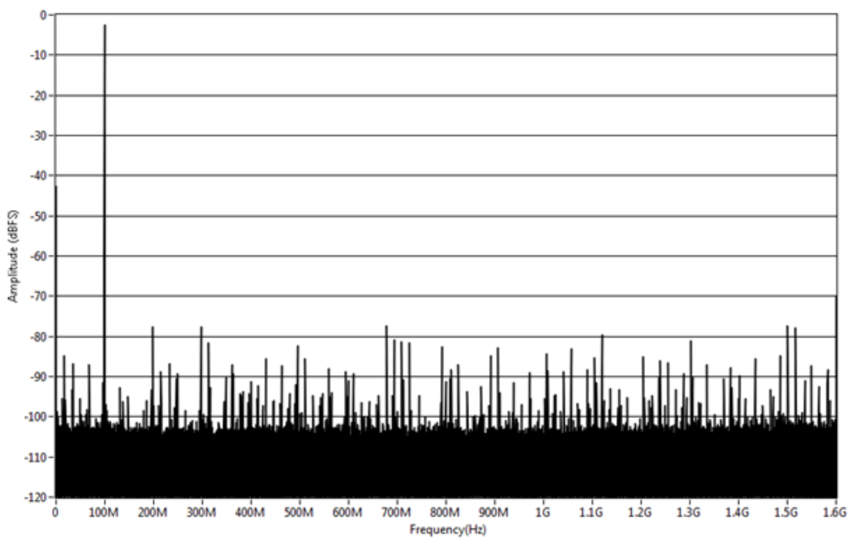


Figure 2. Single Tone Spectrum (Dual Channel Mode, 999 MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01

Variant), Measured

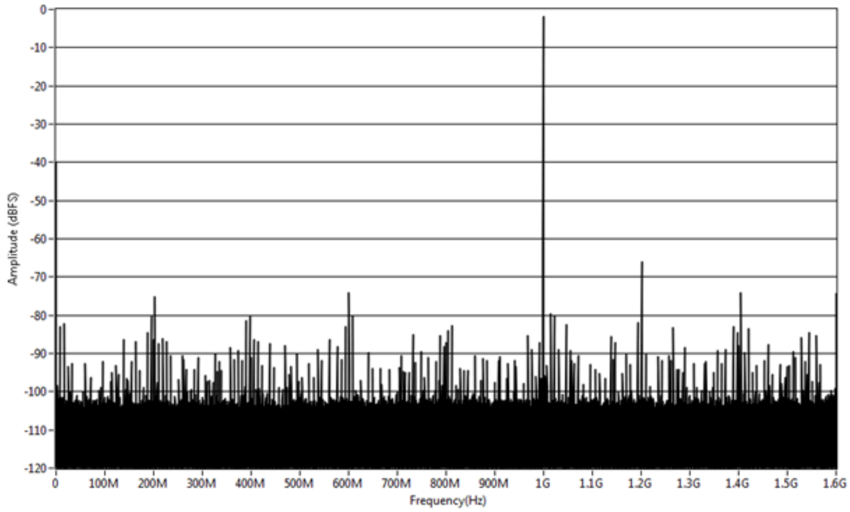


Figure 3. Single Tone Spectrum (Single Channel Mode, 99 MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01 Variant), Measured

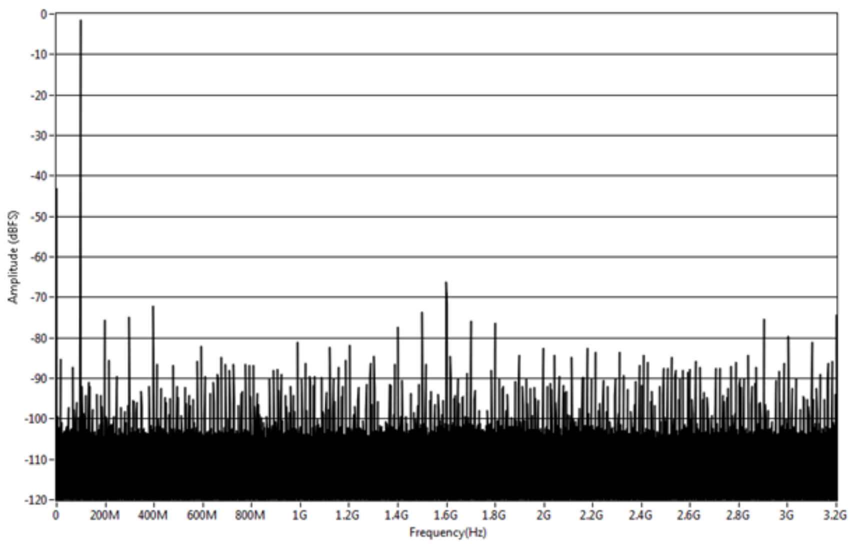
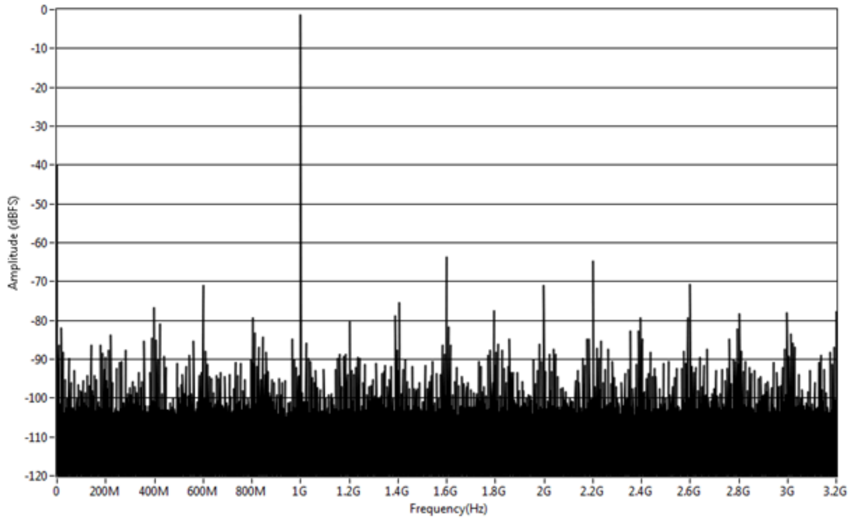


Figure 4. Single Tone Spectrum (Single Channel Mode, 999 MHz, -1 dBFS, 1 V Range, 3.2 kHz RBW, -01

Variant), Measured



Channel-to-channel crosstalk, measured	
99.9 MHz	-94.1 dB
399 MHz	-85.6 dB
999 MHz	-82.5 dB
1.59 GHz	-75.6 dB
1.99 GHz	-72.2 dB

Figure 5. Analog Input Frequency Response (1 V Range, -01 Variant), Measured

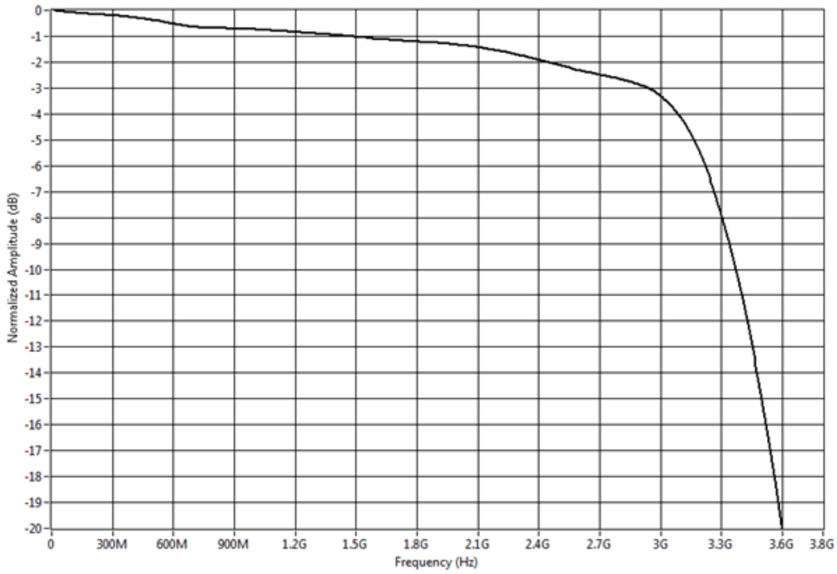


Figure 6. Analog Input Frequency Response (200 mV Range, -01 Variant), Measured

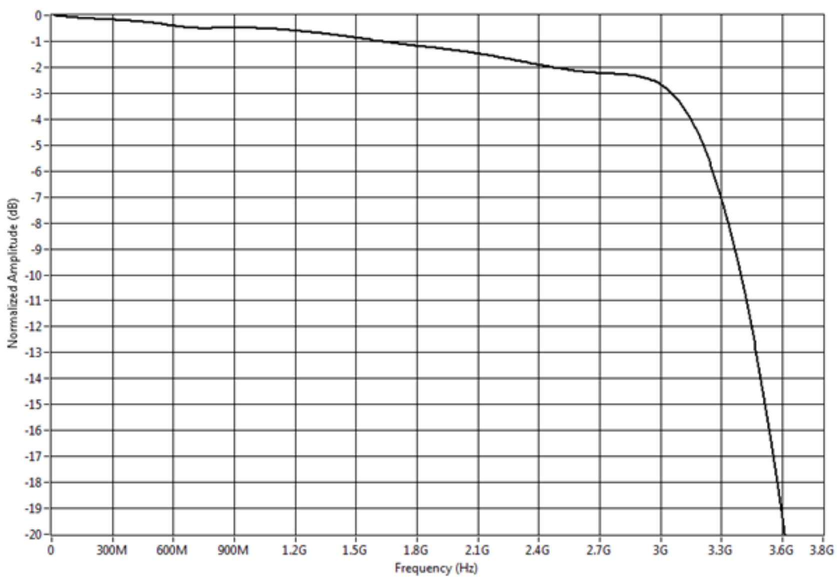


Figure 7. Analog Input Frequency Response (1 V Range, -02 Variant), Measured

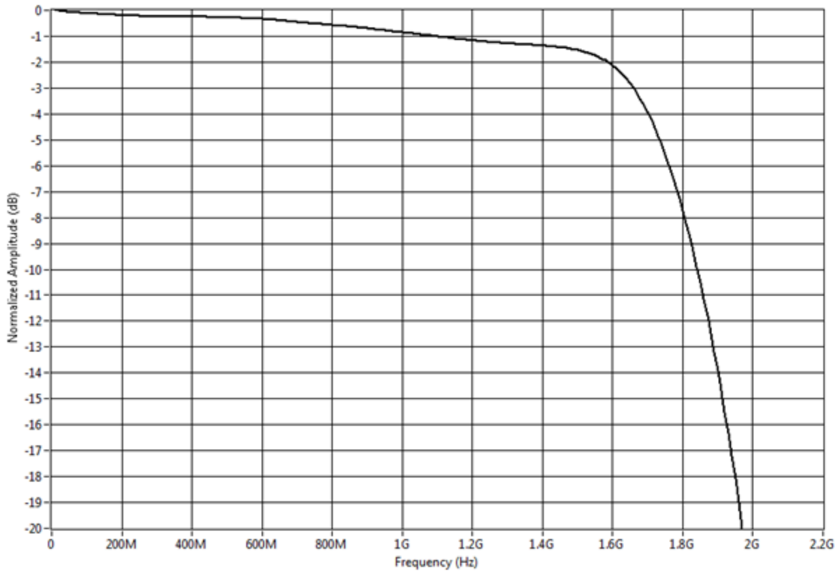


Figure 8. Analog Input Frequency Response (200 mV Range, -02 Variant), Measured

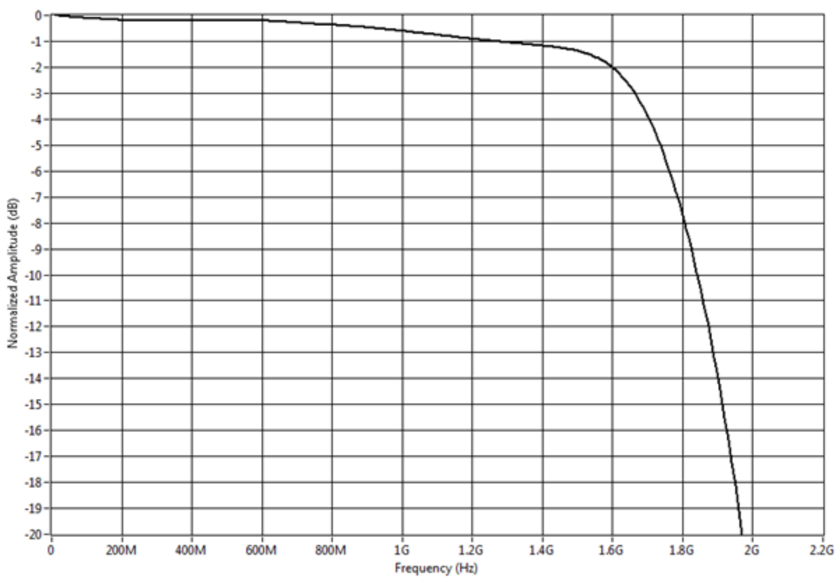


Figure 9. Input Return Loss (1 V Range), Measured

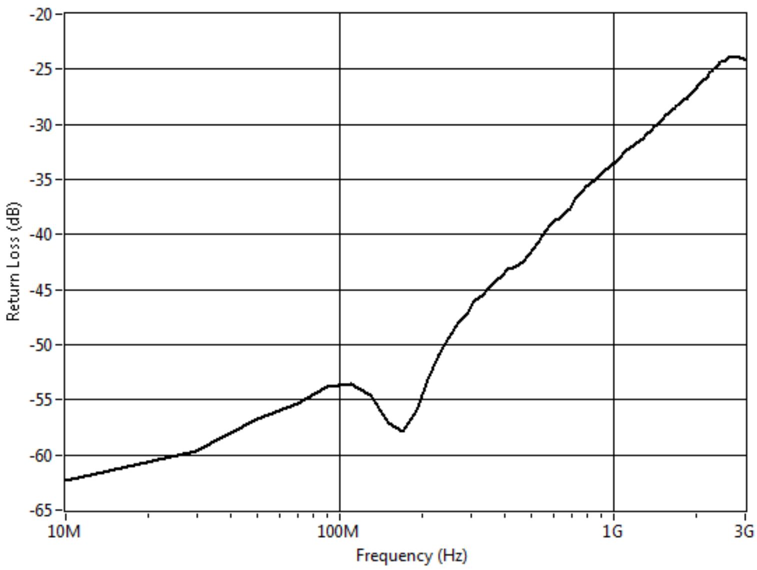
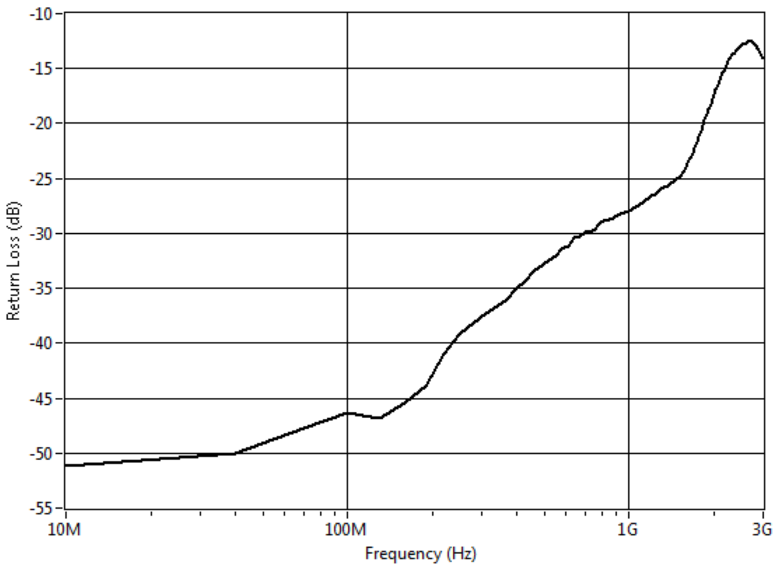


Figure 10. Input Return Loss (200 mV Range), Measured



REF/CLK IN

Connector type	SMA
Input impedance	50 Ω
Input coupling	AC

Input voltage range	0.35 V peak-to-peak to 3.5 V peak-to-peak
Absolute maximum voltage	±12 V DC, 5 V peak-to-peak AC
Duty cycle	45% to 55%
Onboard reference timebase stability	±0.7 ppm
Sample Clock jitter[5]	85 fs RMS, measured

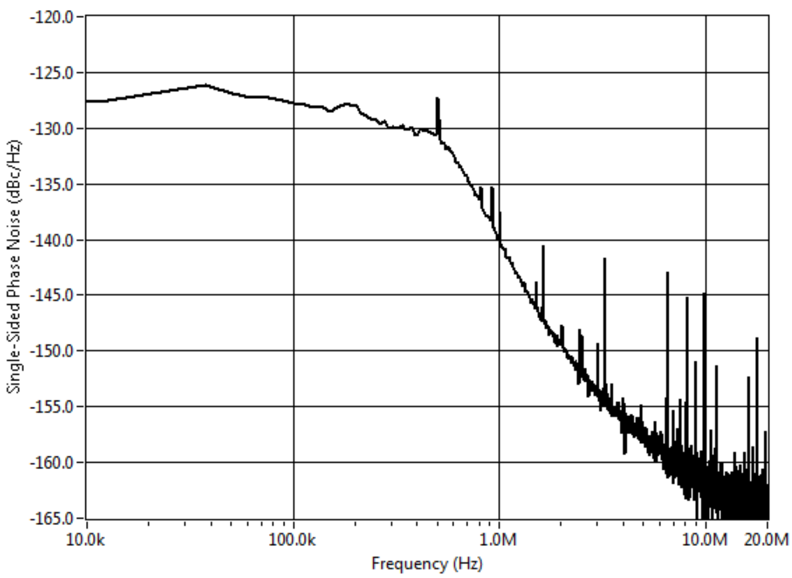
Table 10. Clock Configuration Options

Clock Configuration	External Clock Frequency	Description
Internal Reference Clock*	—	The internal Sample Clock locks to an onboard voltage-controlled temperature compensated crystal oscillator (VCTCXO).
Internal PXI_CLK10	10 MHz	The internal Sample Clock locks to the PXI 10 MHz Reference Clock, which is provided through the FPGA baseboard.
External Reference Clock (REF/CLK IN)	10 MHz †	The internal Sample Clock locks to an external Reference Clock, which is provided through the REF/CLK IN front panel connector.
External Sample Clock (REF/CLK IN)	3.2 GHz	An external Sample Clock can be provided through the REF/CLK IN front panel connector.

5. Integrated from 3.2 kHz to 20 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

Clock Configuration	External Clock Frequency	Description
* Default clock configuration. † The external Reference Clock must be accurate to ±25 ppm.		

Figure 11. Phase Noise with 800 MHz Input Tone, Measured



Analog IN Trigger

Connector type	SMA
Input impedance	50 Ω, nominal
Input coupling	DC
Input voltage range	±5 V

Comparator threshold resolution	12 bits
Minimum pulse width	5 ns
Absolute maximum voltage	±6 V

Digital OUT Trigger

Connector type	SMA
Input impedance	50 Ω, nominal
Input coupling	DC
Logic type	3.3 V CMOS
Maximum current drive	24 mA
Update rate resolution	5 ns
Jitter	3.2 ps RMS, measured

Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	500 g (17.6 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[6]
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g RMS
Nonoperating	5 Hz to 500 Hz, 2.4 g RMS

NI-TClk

You can use the NI-TClk synchronization method and the NI-TClk driver to align the Sample Clocks on any number of supported devices in one or more chassis. For more

6. The PXIe-5774 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the chassis specifications to determine the ambient temperature ranges your chassis can achieve.

information about TClk synchronization, refer to the ***NI-TClk Synchronization Help*** within the ***FlexRIO Help***. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample Clocks of each module.
- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample Clock.

> **Note** Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[7]	80 ps, measured
Skew after manual adjustment	≤10 ps, measured
Sample Clock delay/adjustment	0.4 ps

Skew after manual adjustment	≤10 ps, measured
Sample Clock delay/adjustment	1.5 ps

CableSense

> **Note** NI supports CableSense on the PXIe-5774 with the KU060 FPGA option

7. Caused by clock and analog delay differences. No manual adjustment performed. Tested with a PXIe-1085 chassis with a 24 GB backplane with a maximum slot to slot skew of 100 ps. Measured at 23 °C.

> only.

CableSense pulse voltage[8]	95 mV, nominal
CableSense pulse rise time[9]	550 ps, nominal

Driver support for CableSense on the PXIe-5774 was first available in NI-FlexRIO 20.1.

For more information about CableSense technology, refer to ni.com/cablesense.

8. When measured with a high-impedance device.
9. When sourcing into a 50 Ω cable or load.