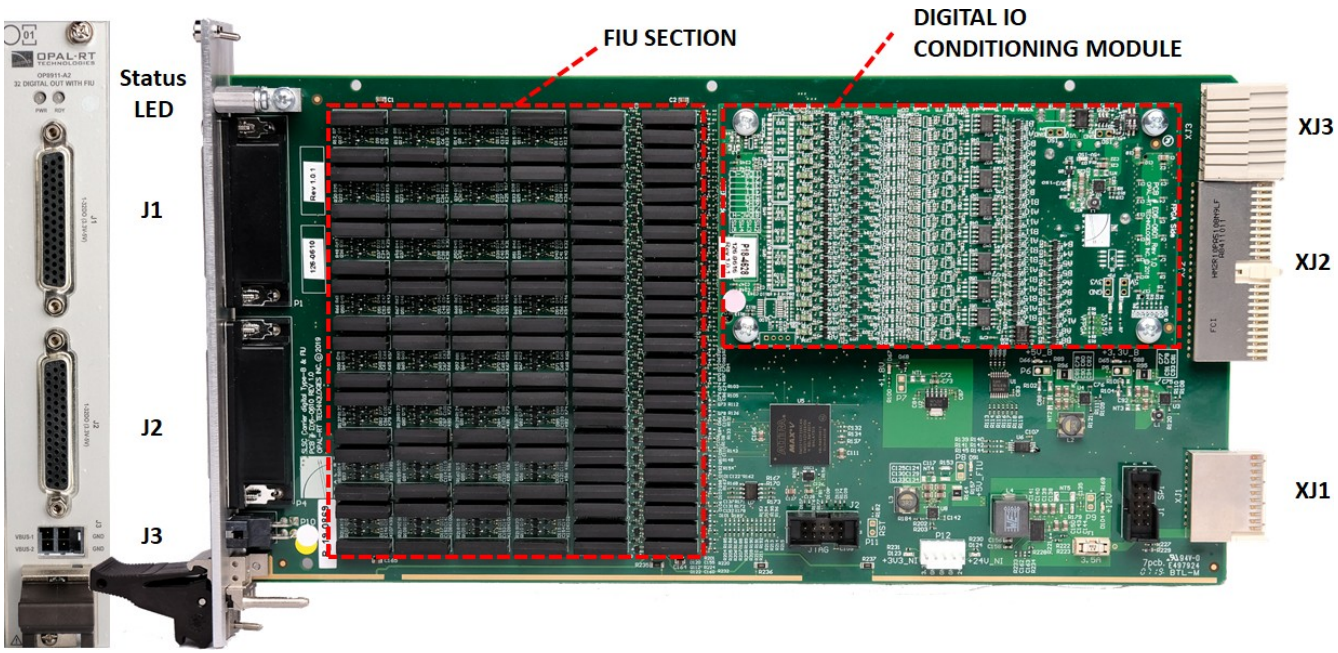
OP8900 SLSC Boards General Information

Form Factor

The SLSC boards are 144.32mm tall (4U) by 281.9mm deep.

Board Layout

Digital Board (OP891x & OP892x)



OP8900 SLSC Boards FIU Description

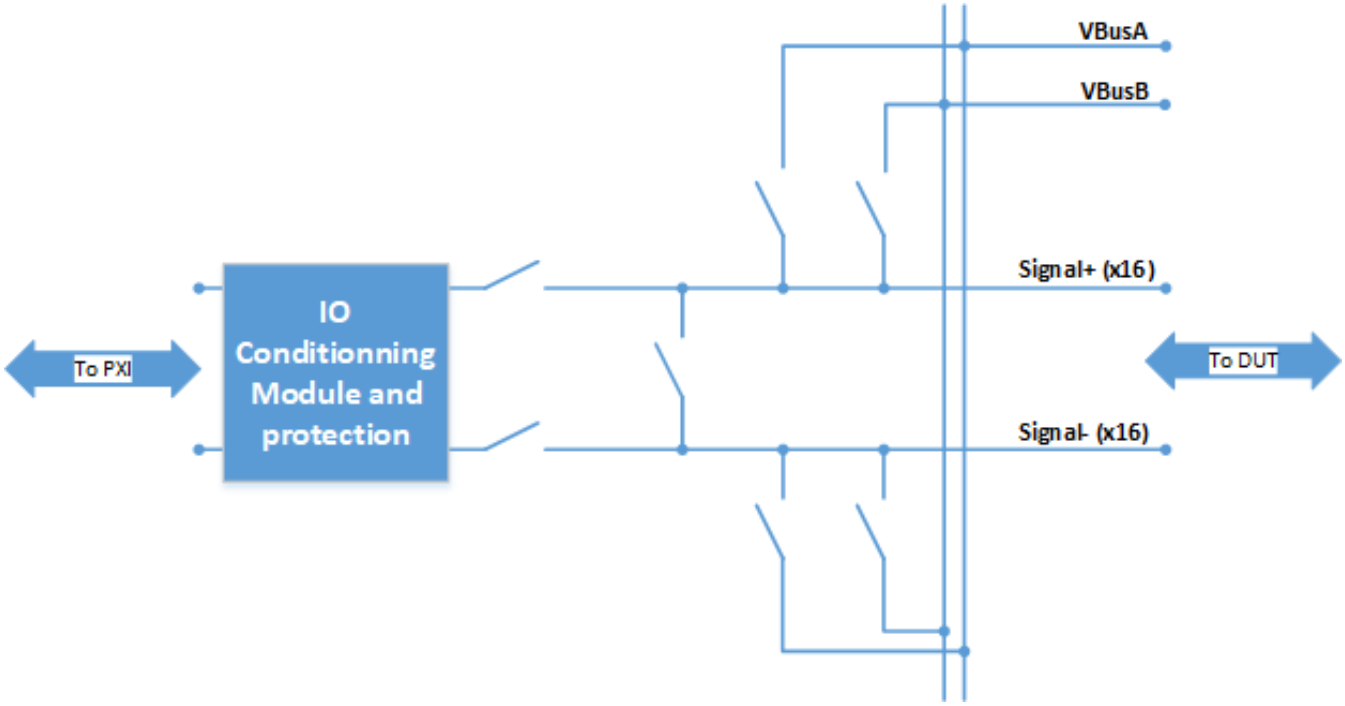
Topology

The Fault Insertion Unit (FIU) section of the OP8900 boards consists of **seven relays per differential pair** of signals, for a total of 112 relays (7 x16).

Each relay can be controlled individually.

For each group of 7 relays, **the possible faults are**

- **Open-circuit** of the pair
- **Short-circuit** of the two signals of the pair
- Two **fault injection**, with two user-supplied voltage references voltages (VBusA and VBusB), for each signal of the pair.



Note: Diagram only shows one channel.

Embedded Protections

The following protections are implemented:

- In the default state, all relays are open
- All channels are updated simultaneously
- VBusA and VBusB cannot be connected on the same channel at the same time: VBusA and VBusB cannot be shorted
- When the Signal + and Signal - are shorted together, only one other fault is allowed for VBusA or VBusB on that channel pair
- Relays on a channel are always open before closing any other

The maximum peak current per relay is 1A. There is no over-current protection

The relay technology used in the FIU allows a higher density and has a fast response time (<0.5ms). However, this technology is very sensitive to peak current, even for a few micro-seconds. It is the customer's responsibility to limit the peak current by adding the resistor on the signal or VBus based on the capacitor and cabling present on the circuit.

Even if the power supply on the VBus is limited to 0.1A, a capacitor is present at the output and the peak current can easily >5A before the internal current limit kick in creating permanent damage to the relay.

If a relay is broken in short mode, an RMA can be issued to repair the card. If the customer has access to a technician with valid IPC-610 certification and experience with a rework of through-hole lead-free and no-clean soldering, OPAL-RT authorizes this technician to replace once a faulty relay.

Here is a short recap of the process:

1. Remove the SLSC card out of the SLSC chassis.
2. With a basic multimeter measure the impedance between pin 1 and 4 of all 112 relays. If <100R, the relay needs to be changed.
3. Unsolder the faulty relay. No-clean flux can be used.
4. Solder a new relay: Comus International 3570-1419-054.

For output signal (analog or digital), always open the load relay (relay in series of the signal) when creating faults to prevent damage on the output circuit.

Even if some protection is built-in on the output circuit to prevent damage, creating a direct fault to VBus with higher voltage can create permanent damage.

OP8910 32 High-Speed Digital IO Conditioning Board

A high-speed DIO board with TTL/LVTTL (5.0V, 3.3V) output and galvanic isolation

OP8910 Description

The OP8910 is a 32 channel digital input/output board with fault insertion as an option, compatible with the NI SLSC-12001 Platform.

Features

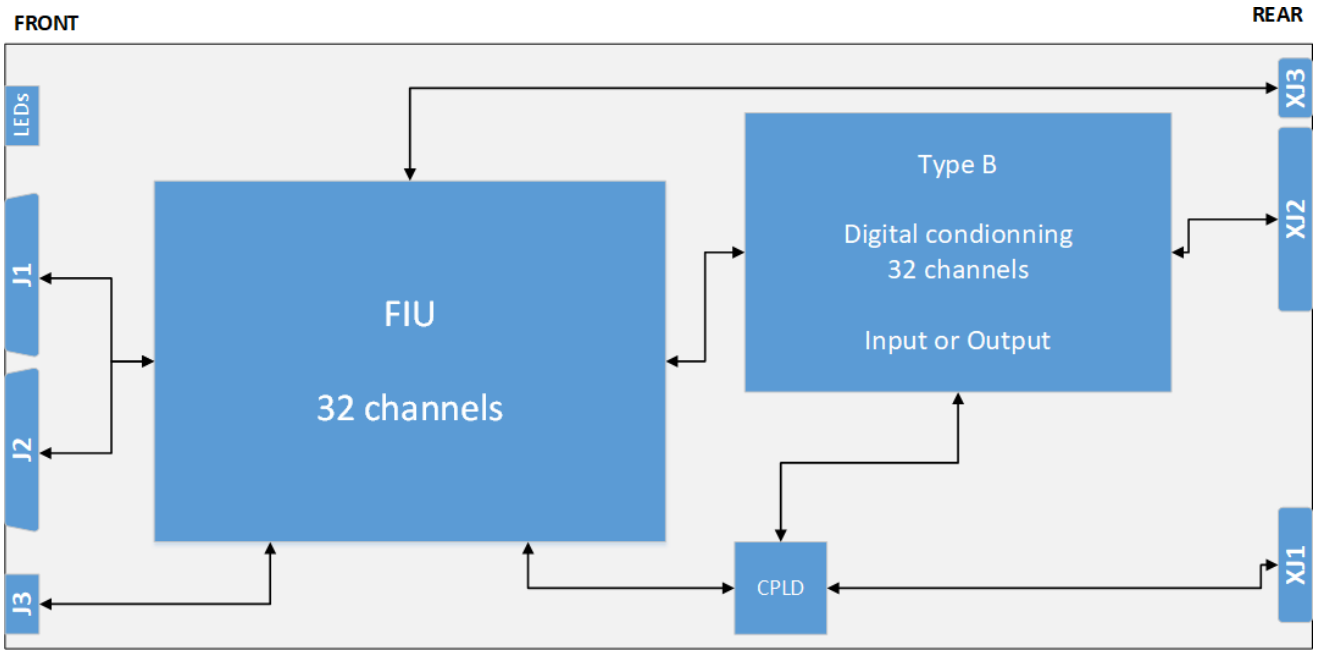
- Signal conditioning & FIU on a single board
- Low latency < 20ns, High resolution of 10ns with 100 MHz FPGA.
- Digital In programmable threshold 0-50V.
- Digital Out TTL, max output current: 32 mA/ch or 800 mA total combined
- Fault insertions module FIU as an option

For a full description of the OP8900 series boards' FIU (fault insertion) unit, see here.

Board Architecture

The board features a combination of 32 input and output channels and a set of relays adding fault insertion capability for each signal.

The general layout of the board is as follows, with the Front Interface connectors on the left and the SLSC backplane connectors on the right:



The input/output conditioning is managed by the Type B OP5367 module.

A CPLD is used to configure the fault insertion unit (FIU) section and the OP5367. It is responsible for the communication of the SLSC card within the NI environment for identification, error reporting, etc. It also receives configuration from the software and applies it to the FIU and to some of the I/Os.

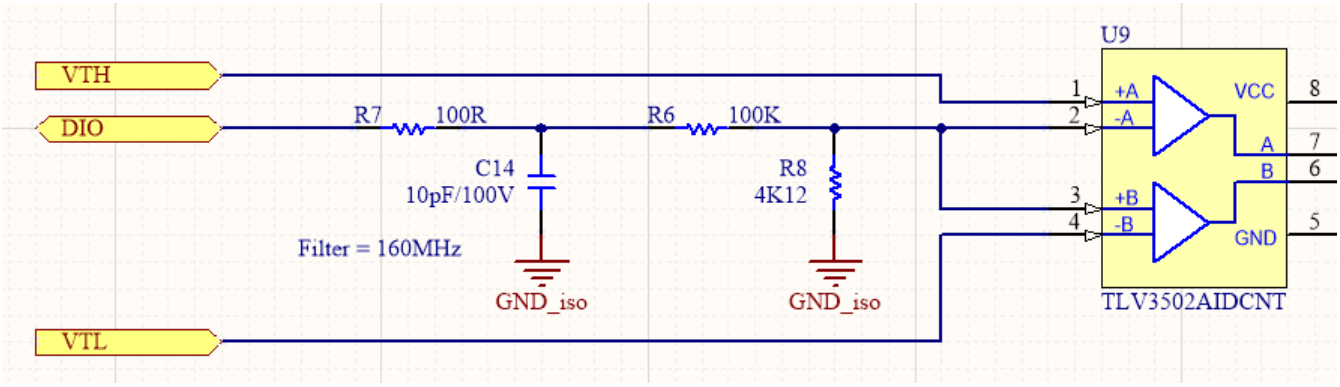
The FIU specification and topology is common to all OP8900 boards.

Channel description

Digital Inputs

The input channels are located on the OP5367 mezzanine. The voltage range is 0 - 50V. Both high and low voltages are programmable per group of 8 channels over the whole range.

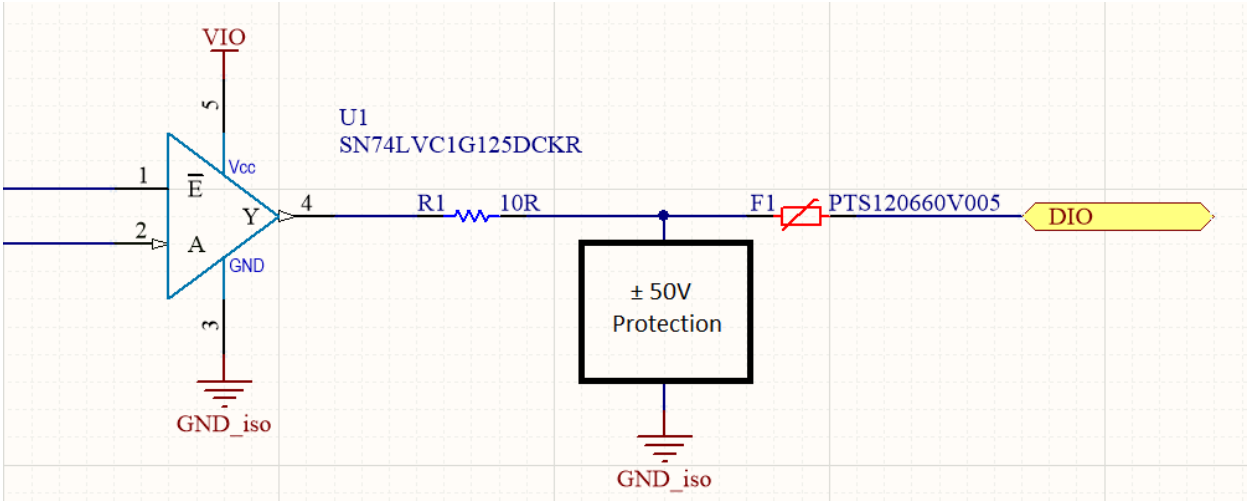
The channels are protected for ±50VDC and ±50VAC.



Digital Outputs

The output channels are located on the OP5367 mezzanine. Their electronic circuit is presented below.

The channels are singled-ended and LVTTL (3.3V) or TTL (5V) compliant (see OP8910 Installation and Configuration for voltage selection) They are protected in case of short-circuits.



Note: Initial values and complementary outputs are not managed by the OP5367.

OP8910 Configurations

Several assemblies of the OP8910 are available, as listed below, with different numbers of inputs and outputs, and with or without the FIU section populated.

Part Number	Description	Digital In	Digital Out	Digital Out Type	FIU
OP8911-F	32 Dout LVTTL/TTL with FIU SLSC Conditioning Board	0	32	TTL	32 single-ended FIU
OP8911-N	32 Dout LVTTL/TTL SLSC Conditioning Board	0	32	TTL	N/A
OP8913-F	16 Din/16 Dout LVTTL/TTL with FIU SLSC Conditioning Board	16	16	TTL	32 single-ended FIU
OP8913-N	16 Din/16 Dout LVTTL/TTL SLSC Conditioning Board	16	16	TTL	N/A
OP8915-F	32 Din with FIU SLSC Conditioning Board	32	0	N/A	32 single-ended FIU
OP8915-N	32 Din SLSC Conditioning Board	32	0	N/A	N/A

OP8910 Installation and Configuration

Installation

The board comes installed with the OP5367 and the FIU relays according to the part number selected.

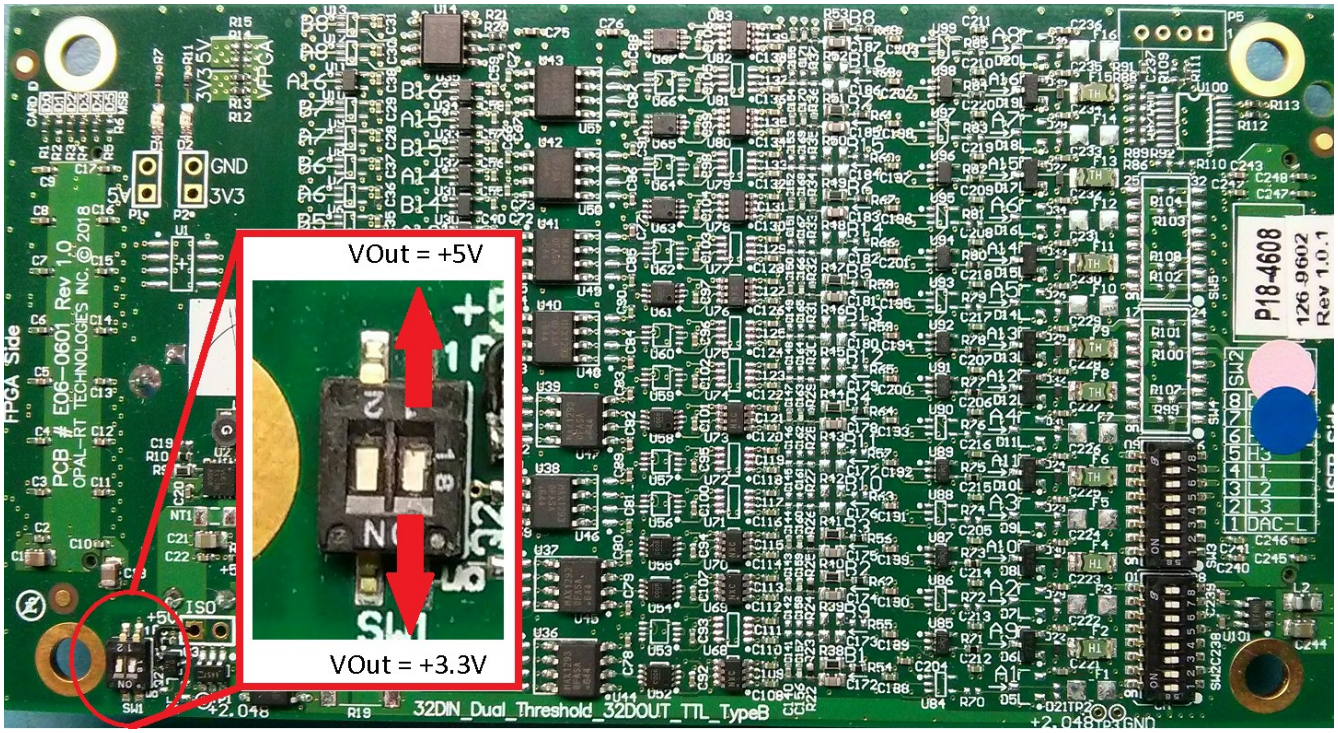
If the board did not come already installed in the NI SLSC-12001 Platform, simply position the module in alignment with the desired slot and push in firmly until the back connectors is pressed into the backplane connectors of the chassis.

Output Voltage Selection

It is possible to select the output voltage of all channels for +3.3V (LVTTL) or +5.0V (TTL) operation via a dipswitch installed on the OP5367.

Make sure the SLSC card is powered down before actioning the dipswitch

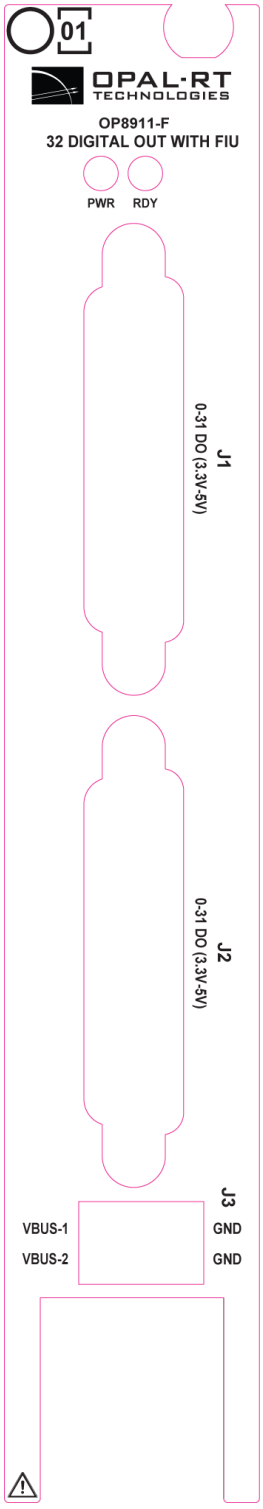
See the location of the dipswitch in the picture below:



OP8910 Hardware Interface

Face plate

The face plate provides two HDB44 connectors (J1, J2), one 4-pin Molex connector (J3) and two LEDs:



J1, J2 Connectors

The 32 digital I/O signals are routed to both J1 and J2 connectors. This allows, for example, splitting the input and output signals into two different cables.

If the harnessing uses only one connector, it is recommended to use J2 (bottom one).

The connectors' pin assignment is detailed in OP8910 Pin assignment

J1-J2 Recommended mating connector

Manufacturer	Part number	Description
Norcomp	180-044-173L000	D-SUB Housings
Norcomp	180-001-170L001	Crimps for 24 to 26 wire gauge
Norcomp	979-025-030R121	

J3 Connector

J3 is used to connect the two external reference voltages for fault insertion.

J3 Mating connector with crimps

Manufacturer	Part number	Description
Molex	538-172258-1004	Headers and Wire Housings
Molex	538-172253-3023-LP	Crimps for 16 to 18 wire gauge

LEDs definition

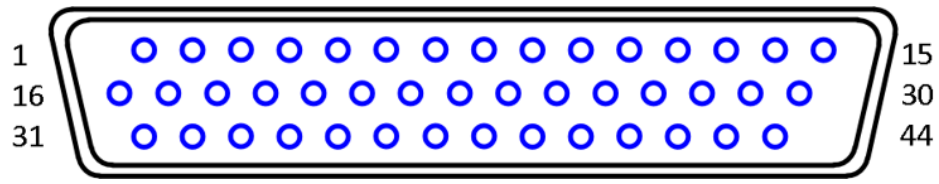
LED Name	LED Behavior	Definition of Behavior
Power	Off	No power present on module (from SLSC Interface nor external power)
	Solid Green	Power Good State
	Blinking Red	Module Fault State
Ready	Off	Module is not powered or in Rdy/Rst# is driven low by the chassis.
	Solid Green	Module in default configuration, recognized by the chassis and ready to configure (The Rdy/Rst# signal has been pulled high by the chassis.)
	Blinking Amber	Module is active (in a non-default configuration and/or communicating with the chassis).

OP8910 Pin Assignment

J1/J2 HDB44 Connector Pinout

As explained in OP8910 Hardware Interface, both HDB44 connectors J1 and J2 share the same pin-out. The 32 digital I/O signals are routed to both J1 and J2 connectors. This allows, for example, splitting the input and output signals into two different cables.

8910 Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Signal Name	D0	D2	D4	GND	D8	D10	D12	NC	D16	D18	D20	GND	D24	D26	D28



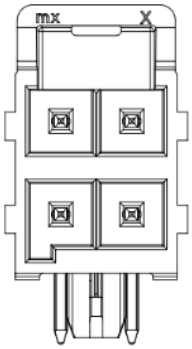
Pin	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Signal Name	D1	D3	D5	GND	D9	D11	D13	NC	D17	D19	D21	GND	D25	D27	D29

Pin	31	32	33	34	35	36	37	38	39	40	41	42	43	44	
Signal Name	D7	D6	GND	GND	D15	D14	GND	GND	D23	D22	GND	GND	D31	D30	

The direction of the signals D0 to D31 depend on the OP8910 assembly selected :

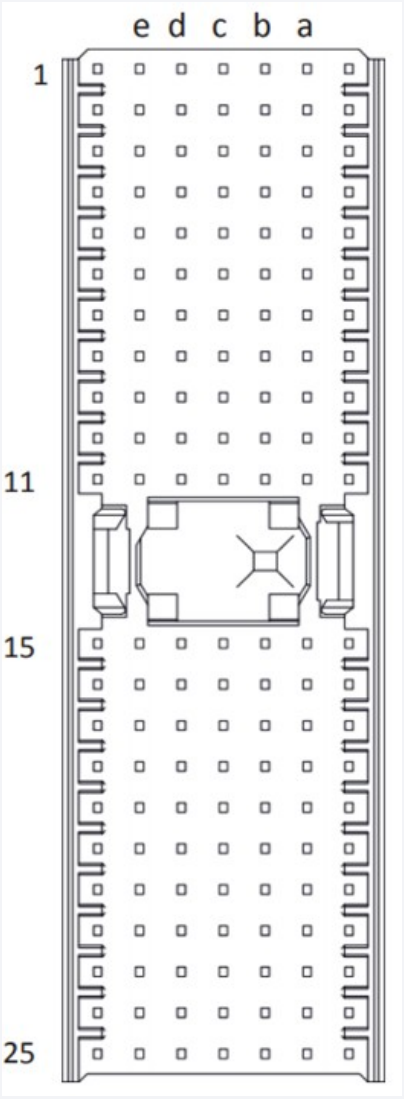
Part Number	Description	Digital In	Digital Out
OP8911	32 Dout LVTTL/TTL SLSC Conditioning Board		D0-D31
OP8913	16 Din/16 Dout LVTTL/TTL SLSC Conditioning Board	D0-D15	D16-D31
OP8915	32 Din SLSC Conditioning Board	D0-D31	

J3 Connector Pinout



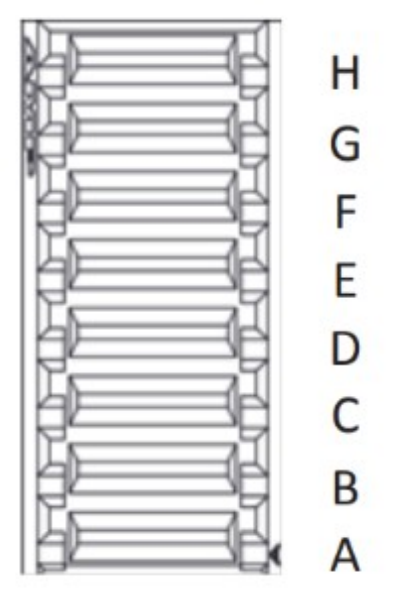
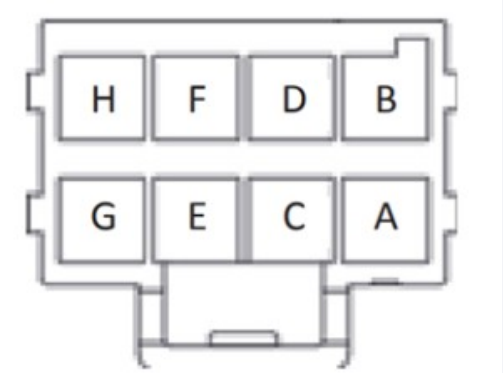
GND_iso	GND_iso
VBus_A	VBus_B

XJ2 Connector Pinout



XJ2 Signal	OP8910	XJ2 Pin	XJ2 Signal	OP8910	XJ2 Pin
P0.0	**D0**	a1	P2.0	**D16**	a7
P0.1	**D1**	b1	P2.1	**D17**	b7
P0.2	**D2**	d1	P2.2	**D18**	d7
P0.3	**D3**	e1	P2.3	**D19**	e7
P0.4	**D4**	a2	P2.4	**D20**	a8
P0.5	**D5**	b2	P2.5	**D21**	b8
P0.6	**D6**	d2	P2.6	**D22**	d8
P0.7	**D7**	e2	P2.7	**D23**	e8
GND	GND	a3	GND	GND	a9
GND	GND	b3	GND	GND	b9
GND	GND	c3	GND	GND	c9
GND	GND	d3	GND	GND	d9
GND	GND	e3	GND	GND	e9
P1.0	**D8**	a4	P3.0	**D24**	a10
P1.1	**D9**	b4	P3.1	**D25**	b10
P1.2	**D10**	d4	P3.2	**D26**	d10
P1.3	**D11**	e4	P3.3	**D27**	e10
P1.4	**D12**	a5	P3.4	**D28**	a11
P1.5	**D13**	b5	P3.5	**D29**	b11
P1.6	**D14**	d5	P3.6	**D30**	d11
P1.7	**D15**	e5	P3.7	**D31**	e11
GND	GND	a6	GND	GND	a20
GND	GND	b6	GND	GND	b20
GND	GND	c6	GND	GND	c20
GND	GND	d6	GND	GND	d20
GND	GND	e6	GND	GND	e20
GND	GND	a17	GND	GND	a23
GND	GND	b17	GND	GND	b23
GND	GND	c17	GND	GND	c23
GND	GND	d17	GND	GND	d23
GND	GND	e17	GND	GND	e23

XJ3 Connector Pinout

XJ3 connector	Molex connector (on standard RTI)	XJ3 pin	OP8910
		**H**	VBus_A
		G	GND_iso
		F	VBus_B
		E	GND_iso
		D	VUser_1
		C	GND_iso
		B	VUser_2
		A	GND_iso

OP8910 Specification

General

Product Name	**OP8910**
Part Numbers	see OP8910 configurations options
Board Type	Digital input/output conditioning
Form Factor	SLSC
SLSC Module Design Specifications	Version 1.2.1
SLSC Compliance Level	1
Rear I/O Compatibility	[01] (Digital Input/Output up to 32 channels)
Hot-Plug support	No

Characteristics

Number of channels	32 input or output channels Number of input /outputs depend on assembly selected. See OP8910 configurations options
Max peak current with FIU	1A, see OP8900 SLSC Boards - FIU Description
Digital Inputs	
• Voltage Range	0-50V with programmable high/low threshold on the whole voltage range, per group of 8
• Protection	±50VDC and ±50VAC
• Input Impedance	> 100kOhms
Digital Outputs	
• Type	Single-ended outputs
• Voltage Range	3.3V or 5.0V (LVTTL, TTL)

• Protection	Short Circuit Protection Protection limit: ±50VDC and ±50VAC, for single or multiple faults
• Current limit	32mA/ch, 800 mA total
• Output impedance	25 Ohms

Dynamic Characteristics

Maximum Frequency	>100Mb/s
Latency	<20ns
Timing Resolution	12.5ns (for FPGA at 80MHz), 10ns (for FPGA at 100MHz)

Environmental

The OP8910 is designed for **indoor use only.**

Module operating temperature	0 °C to 85 °C
Storage temperature	-40 °C to 85 °C
Operating humidity	10% to 90% non-condensing
Storage humidity	5% to 95% non-condensing
Pollution Degree	2
Maximum altitude	2,000 m
Power requirement	12W