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# PCI-5152

# Specifications

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2025-03-14



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# PCI-5152 Specifications

## Definitions

**Warranted** specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. **Warranted** specifications account for measurement uncertainties, temperature drift, and aging. **Warranted** specifications are ensured by design or verified during production and calibration.

**Characteristics** describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications in this document are **Typical** unless otherwise noted.

## Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 1 GS/s
- Real-Time Interleaved Sampling (TIS) mode provides a 2 GS/s real-time sample rate for a single channel
- The module is warmed up for 15 minutes at ambient temperature
- Self-calibration is completed after warm-up period
- Calibration cycle is maintained

- The PXI/PCI chassis fan speed is set to HIGH, the foam fan filters are removed (if present), and the empty slots contain chassis slot blockers and filler panels. For more information about cooling, refer to **Note to Users: Maintain Forced Air Cooling** on ni.com.

## Vertical

### Analog Input (Channel 0 and Channel 1)

Number of channels	Two (simultaneously sampled)
Connectors	BNC

### Impedance and Coupling

Input Impedance (software-selectable)		
50 $\Omega$	50 $\Omega$ $\pm$ 1.5%	
1 M $\Omega$	1 M $\Omega$ $\pm$ 0.75% in parallel with a nominal capacitance of 22 pF	
Input coupling	Software-selectable: AC, DC, GND	

### Voltage Levels

**Table 1.** Full Scale (FS) Input Range and Programmable Vertical Offset Range

Range ( $V_{pk-pk}$ )	50 $\Omega$ Offset (V)	1 M $\Omega$ Offset (V)
0.1	$\pm$ 1	$\pm$ 1
0.2		
0.4		

Range ( $V_{pk-pk}$ )	50 $\Omega$ Offset (V)	1 M $\Omega$ Offset (V)
1		
2	$\pm 6$	$\pm 10$
4	$\pm 5$	
10	$\pm 2$	

Maximum input overload	
50 $\Omega$	7 $V_{rms}$ with $ Peaks  \leq 10$ V
1 M $\Omega$	$ Peaks  \leq 42$ V

## Accuracy

Resolution	8 bits
DC accuracy, warranted <sup>[1][2]</sup>	
0.1 V to 1 V input range	$\pm(1.26\% \text{ of Input} + 1.0\% \text{ of FS} + 500 \mu\text{V})$
2 V to 10 V input range	$\pm(1.26\% \text{ of Input} + 1.0\% \text{ of FS} + 5 \text{ mV})$
Programmable vertical offset accuracy <sup>[2]</sup>	$\pm 0.9\% \text{ of offset setting, warranted}$
DC Drift, nominal <sup>[3]</sup>	
0.1 V to 1 V input range	$\pm(0.052\% \text{ of Input} + 100 \mu\text{V}) \text{ per } ^\circ\text{C}$

2 V to 10 V input range	$\pm(0.052\% \text{ of Input} + 1.0 \text{ mV}) \text{ per } ^\circ\text{C}$
<b>Crosstalk</b>	
<b>CH 0 to/from CH 1<sup>[4]</sup></b>	
10 MHz	<-80 dB
100 MHz	<-60 dB
<b>Ext Trig to CH 0 or CH 1<sup>[5]</sup></b>	
10 MHz	<-80 dB
100 MHz	<-80 dB

## Bandwidth and Transient Response

<b>Bandwidth (-3 dB), warranted<sup>[6], [7]</sup></b>	
<b>0.1 V input range</b>	
50 $\Omega$	165 MHz, typical 135 MHz minimum
1 M $\Omega$	135 MHz, typical 110 MHz minimum
<b>All other input ranges</b>	
50 $\Omega$	340 MHz, typical

	300 MHz minimum
1 M $\Omega$	300 MHz, typical 260 MHz minimum
<b>Rise/fall time</b> <sup>[8]</sup>	
<b>0.1 V input range</b>	
50 $\Omega$	2.4 ns
1 M $\Omega$	2.8 ns <sup>[9]</sup>
<b>All other input ranges</b>	
50 $\Omega$	1.2 ns
1 M $\Omega$	1.4 ns <sup>[9]</sup>
Bandwidth limit filter	20 MHz noise filter
<b>AC coupling cutoff (-3 dB)</b> <sup>[10]</sup>	
50 $\Omega$	106 kHz
1 M $\Omega$	12 Hz

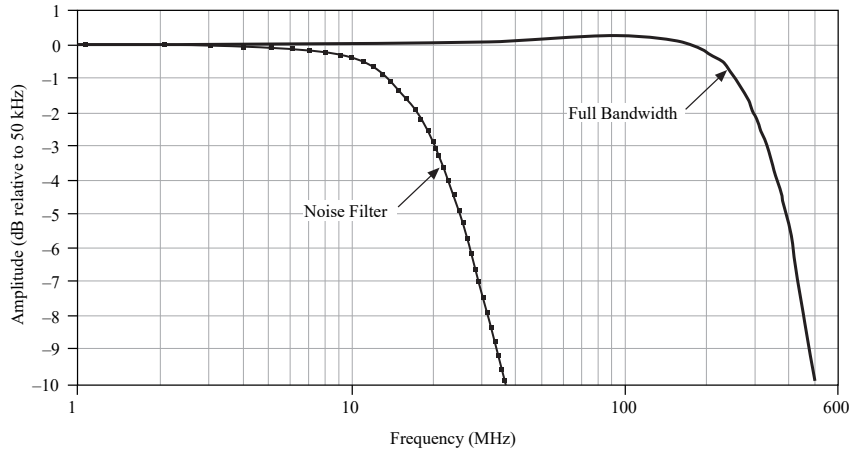
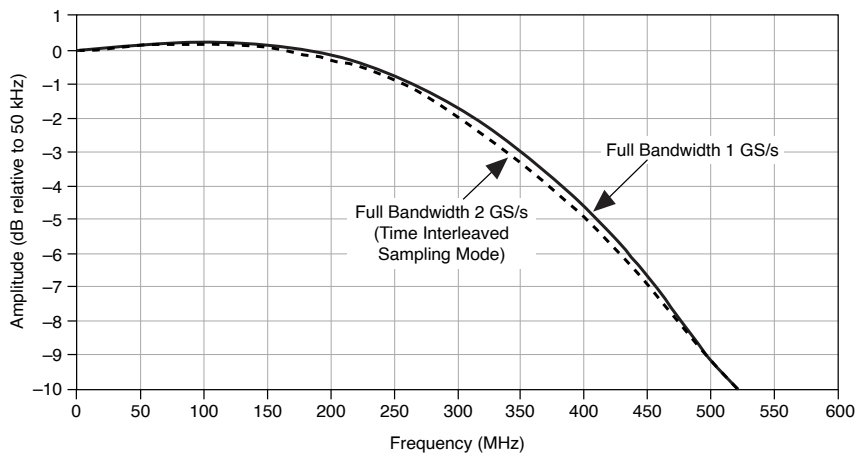
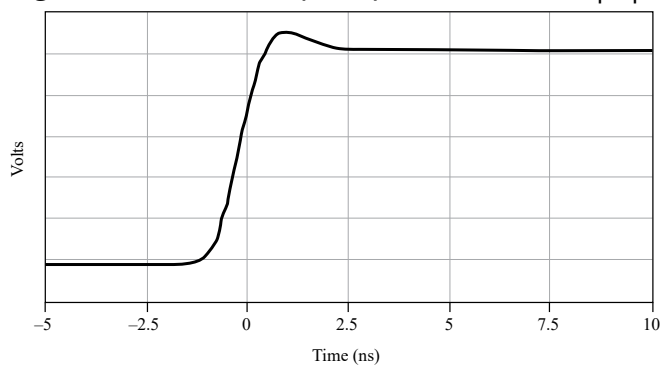
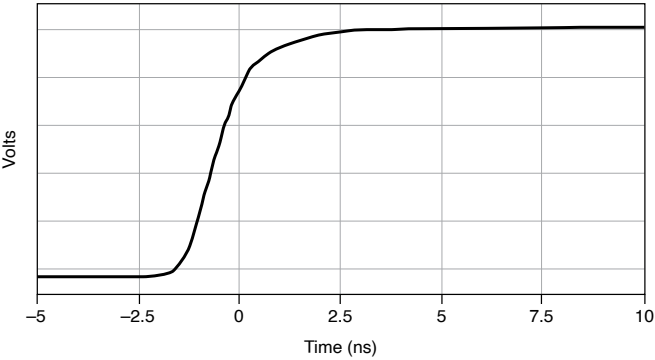
**Figure 1.** PCI-5152 Frequency Response, 50  $\Omega$ , 1 V, Measured**Figure 2.** PCI-5152 Frequency Response, 50  $\Omega$ , 1 V Input Range, Measured**Figure 3.** PCI-5152 Step Response, 50  $\Omega$ , 10 V<sub>pk-pk</sub> through 0.2 V<sub>pk-pk</sub> Input Range, Measured



Figure 4. PCI-5152 Step Response, 50  $\Omega$ , 0.1 V<sub>pk-pk</sub> Input Range, Measured



Spectral Characteristics

ENOB <sup>[11]</sup>	
Noise filter on	7.3
Noise filter off	7.1
Signal to Noise and Distortion (SINAD) <sup>[11]</sup>	
Noise filter on	45 dB
Noise filter off	43 dB

Figure 5. PCI-5152 Dynamic Performance, 50  $\Omega$ , 1 V<sub>pk-pk</sub> Range, 9.425 MHz, -1 dBFS Input Signal, Measured

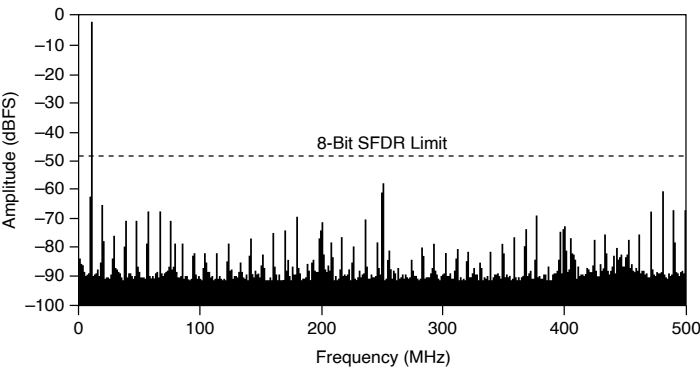
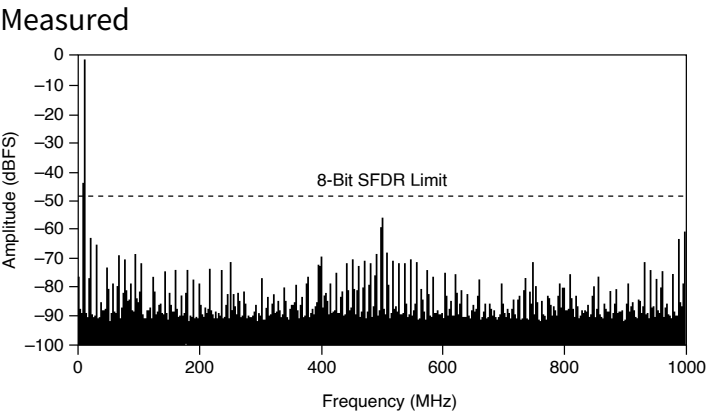


Figure 6. PCI-5152 TIS Dynamic Performance, 50  $\Omega$ , 1 V<sub>pk-pk</sub> Range, 9.425 MHz, -1 dBFS Input Signal,



Noise

Table 2. RMS Noise<sup>[12]</sup>

Range (V <sub>pk-pk</sub> )	Noise Filter On	Noise Filter Off
0.1	240 $\mu$ V <sub>rms</sub> (0.24% FS)	320 $\mu$ V <sub>rms</sub> (0.32% FS)
0.2	480 $\mu$ V <sub>rms</sub> (0.24% FS)	600 $\mu$ V <sub>rms</sub> (0.30% FS)
0.4	960 $\mu$ V <sub>rms</sub> (0.24% FS)	1.12 mV <sub>rms</sub> (0.28% FS)
1	2.4 mV <sub>rms</sub> (0.24% FS)	2.6 mV <sub>rms</sub> (0.26% FS)
2	4.8 mV <sub>rms</sub> (0.24% FS)	6.0 mV <sub>rms</sub> (0.30% FS)
4	9.6 mV <sub>rms</sub> (0.24% FS)	11.2 mV <sub>rms</sub> (0.28% FS)
10	24 mV <sub>rms</sub> (0.24% FS)	26 mV <sub>rms</sub> (0.26% FS)

Channel-to-channel skew	<100 ps
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Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCSO) <sup>[13]</sup>

External	PFI 0 (front panel SMB connector)
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## Onboard Clock (Internal VCSO)

Sample rate range	
Real-time sampling (single shot) <sup>[14]</sup>	15.26 kS/s to 1 GS/s
TIS <sup>[15]</sup> mode (single shot)	2 GS/s (single channel only)
Random interleaved sampling (RIS) mode <sup>[16]</sup>	2 GS/s to 20 GS/s in increments of 1 GS/s (repetitive waveforms only)
Timebase accuracy	
Not phase-locked to Reference clock	$\pm 30$ ppm within $\pm 3$ °C of external calibration temperature, plus an additional $\pm 7$ ppm per °C outside of $\pm 3$ °C of external calibration temperature, warranted
Phase-locked to Reference clock	Equal to the Reference clock accuracy <sup>[17]</sup>
Sample clock delay range	$\pm 1$ Sample clock period
Sample clock delay/adjustment resolution	$\leq 5$ ps

## External Sample Clock

Sources	PFI 0 (front panel SMB connector)
Frequency range <sup>[18]</sup>	350 MHz to 1 GHz
Duty cycle tolerance	45% to 55%

## Phase-Locked Loop (PLL) Reference Clock

Sources	RTSI 7 PFI 0 (front panel SMB connector)
Frequency range <sup>[19]</sup>	1 MHz to 20 MHz, in 1 MHz increments Default: 10 MHz
Duty cycle tolerance	45% to 55%
Exported Reference clock destinations	RTSI <0..7> PFI 1 (front panel SMB connector)

## Sample Clock and Reference Clock Input (PFI 0, Front Panel Connector)

Input voltage range	Sine wave: 0.65 V <sub>pk-pk</sub> to 2.8 V <sub>pk-pk</sub>
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	(0 dBm to 13 dBm)
Maximum input overload	7 V RMS with $ Peaks  \leq 10$ V
Impedance	50 $\Omega$
Coupling	AC

## Reference Clock Output (PFI 1, Front Panel Connector)

Output impedance	50 $\Omega$
Logic type	3.3 V CMOS, except when exporting 5 V
Maximum drive current	$\pm 24$ mA

## Trigger

Trigger types <sup>[20]</sup>	Edge
	Window
	Hysteresis
	Video
	Digital
	Immediate

	Software
Trigger sources	CH 0 CH 1 TRIG PFI <0..1> RTSI <0..6> Software
<b>Time resolution</b>	
Onboard clock, time-to-digital conversion circuit (TDC) on	5 ps
Onboard clock, TDC off	1 ns
External clock, TDC off	External clock period
<b>Minimum rearm time</b> <sup>[21]</sup>	
TDC on	8 μs
TDC off	1 μs
Holdoff	From rearm time up to $[(2^{32} - 1) \times \textbf{Sample Clock Period}]$
Trigger delay	From 0 up to $[(2^{35} - 1) - \textbf{Posttrigger Samples}] \times (1 / \textbf{Sample Rate})$ , in seconds

## Analog Trigger

Trigger types	Edge
	Window
	Hysteresis
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)
Trigger level range <sup>[22]</sup>	
CH 0, CH 1	100% FS
TRIG (External trigger)	±5 V
Voltage resolution	8 bits (1 in 256)
Trigger level accuracy <sup>[23]</sup>	
CH 0, CH 1	±5% FS up to 10 MHz, warranted
TRIG (External trigger)	±1 V (±10% FS) up to 10 MHz, warranted
Edge trigger sensitivity <sup>[22]</sup> , warranted	
CH 0, CH 1	10% FS

TRIG (External trigger)		1.0 Vpp
Trigger jitter <sup>[23]</sup>	≤10 ps <sub>rms</sub> , typical	
	≤20 ps <sub>rms</sub> , maximum	
Trigger filters		
Low frequency reject (LF)		50 kHz
High frequency reject (HF)		50 KHz

## Digital Trigger

Trigger type	Digital
Sources	RTSI <0..6> PFI <0..1> (front panel SMB connector)

## External Trigger Input (Front Panel Connector)

Connector	BNC
Impedance	1 M $\Omega$ in parallel with a nominal capacitance of 22 pF
Coupling	AC, DC



AC coupling cutoff (-3 dB)	12 Hz
Input voltage range	$\pm 5$ V
Maximum input overload	Peaks  $\leq 42$ V

## PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Connector	SMB jack
Direction	Bidirectional

## As an Input (Trigger)

Destination	Start trigger (acquisition arm) Reference (stop) trigger Arm reference trigger Advance trigger
Input impedance	150 k $\Omega$ , nominal
V <sub>IH</sub>	2.0 V

$V_{IL}$	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz

## As an Output (Event)

Sources	Start trigger (acquisition arm) Reference (stop) trigger End of record Done (end of acquisition) Probe compensation <sup>[24]</sup>
Output impedance	50 $\Omega$
Logic type	3.3 V CMOS
Maximum drive current	$\pm 24$ mA
Maximum frequency	25 MHz

# Waveform Specifications

**Table 3. Onboard Memory Size**

Real-Time and RIS Modes	Real-Time TIS Mode
8 MB standard (8 MS) per channel	8 MB standard (8 MS)
64 MB option (64 MS) per channel	64 MB option (64 MS)
256 MB option (256 MS) per channel	256 MB option (256 MS)
—	512 MB option (512 MS)

Minimum record length	1 sample	
Number of pretrigger samples	Zero up to full record length	
Number of posttrigger samples	Zero up to full record length	
Maximum number of records in onboard memory <sup>[26]</sup>		
8 MB per channel	32,768	
64 MB per channel	100,000	
256 MB per channel	100,000	
512 MB per channel	100,000	
Allocated onboard memory	[(Record length × 1 byte/sample) + 400 bytes] rounded up to next	

per record	multiple of 128 bytes
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# Calibration

## External Calibration

External calibration calibrates the VCISO and the voltage reference. All calibration constants are stored in nonvolatile memory.

## Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, triggering, and timing errors for all input ranges.

## Calibration Specifications

Interval for external calibration	2 years
Warm-up time <sup>[27]</sup>	15 minutes

# Software

## Driver Software

Driver support for the PCI-5152 was first available in NI-SCOPE 3.3.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-5152. NI-SCOPE provides application programming interfaces for many development environments.

## Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

## Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PCI-5152 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.



**Note** InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE-specific soft front panel instead of InstrumentStudio.

Interactive control of the PCI-5152 was first available via InstrumentStudio in NI-SCOPE and via the NI-SCOPE SFP in NI-SCOPE3.3. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PCI-5152. MAX is included on the driver media.

## TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the ***NI-TClk Synchronization***

**Help**, which is located within the **NI High-Speed Digitizers Help**. For other configurations, including multichassis systems, contact NI Technical Support at [ni.com/support](https://ni.com/support).

### Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one NI PXI-1042 chassis
- The NI-TClk driver is used to align the Sample clocks of each module
- All parameters are set to identical values for each module
- Modules are synchronized without using an external Sample clock
- Sample clock set to 1 GS/s and all filters are disabled



**Note** Although you can use NI-TClk to synchronize non-identical SMC-based modules, these specifications apply only to synchronizing identical modules.

Skew	500 ps
Skew after manual adjustment	≤5 ps
Sample clock delay/adjustment resolution	≤5 ps

## Power

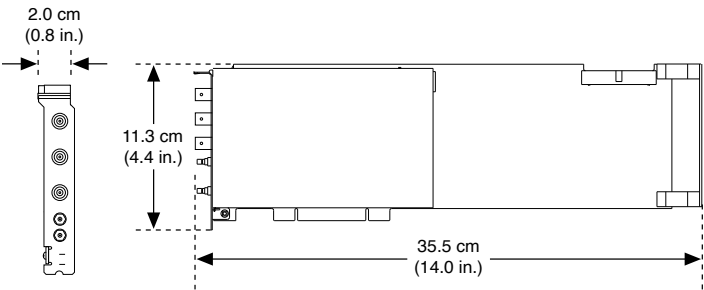
Current draw	
+3.3 VDC	2.5 A
+5 VDC	2.4 A

+12 VDC	200 mA
-12 VDC	0 A
Total power	22.65 W

Physical

Dimensions	35.5 cm x 2.0 cm x 11.3 cm (14.0 in x 0.8 in x 4.4 in)
Weight	445 g (15.7 oz)

Figure 7. PCI-5152 Dimensions



Environment

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

### Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

### Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

## Compliance and Certifications

### Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1



**Note** For safety certifications, refer to the product label or the [Product Certifications and Declarations](#) section.

### Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical



equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



**Note** In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



**Note** Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



**Note** For EMC declarations, certifications, and additional information, refer to the [Product Certifications and Declarations](#) section.

## Product Certifications and Declarations


Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit [ni.com/product-certifications](https://ni.com/product-certifications), search by model number, and click the appropriate link.

## Environmental Management


NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at [ni.com/environment](https://ni.com/environment). This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

#### EU and UK Customers

-  **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit [ni.com/environment/weee](https://ni.com/environment/weee).

#### 电子信息产品污染控制管理办法（中国RoHS）

-  **中国RoHS**—NI符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于NI中国RoHS合规性信息，请登录 [ni.com/environment/rohs\\_china](https://ni.com/environment/rohs_china)。(For information about China RoHS compliance, go to [ni.com/environment/rohs\\_china](https://ni.com/environment/rohs_china).)