PXIe-7899 Specifications

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Contents

PXIe-7899 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

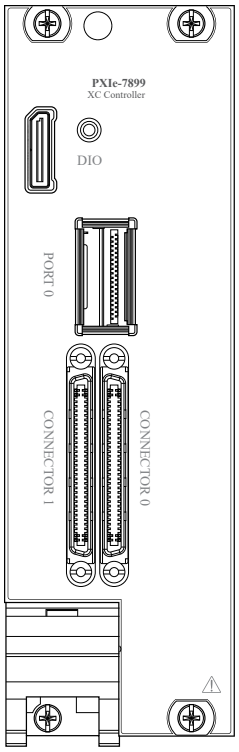
Specifications are ***Typical*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C
- Installed in chassis with slot cooling capacity ≥58 W

PXIe-7899 Front Panel



Connector Pinouts

Figure 1. Digital I/O (DIO) Connector

Reserved	A1	B1	5 V
GND	A2	B2	GND
MGT Rx+ 0	A3	B3	MGT Tx+ 0
MGT Rx– 0	A4	B4	MGT Tx– 0
GND	A5	B5	GND
MGT Rx+ 1	A6	B6	MGT Tx+ 1
MGT Rx– 1	A7	B7	MGT Tx– 1
GND	A8	B8	GND
DIO 4	A9	B9	DIO 6
DIO 5	A10	B10	DIO 7
GND	A11	B11	GND
DIO 0	A12	B12	DIO 2
DIO 1	A13	B13	DIO 3
GND	A14	B14	GND
MGT Rx+ 2	A15	B15	MGT Tx+ 2
MGT Rx– 2	A16	B16	MGT Tx– 2
GND	A17	B17	GND
MGT Rx+ 3	A18	B18	MGT Tx+ 3
MGT Rx– 3	A19	B19	MGT Tx– 3
GND	A20	B20	GND
5.0 V	A21	B21	Reserved

Table 1. Pin Descriptions for DIO Connector

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Notice The maximum input signal levels are valid only when the module is powered on. To avoid permanent damage to the PXIe-7899, do not apply a signal to the device when the module is powered down.

Notice Connections that exceed any of the maximum ratings of any connector on the PXIe-7899 can damage the device and the system. NI is not liable for any damage resulting from such connections.

Figure 2. PORT 0 Connector

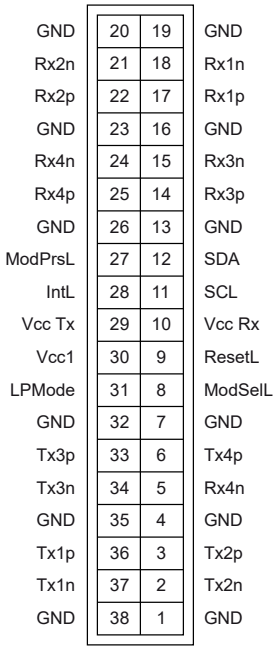


Table 2. Pin Descriptions for PORT 0 Connector

Symbol	Signal Name
Txn <1..4>	Transmitter Inverted Data Input
Txp <1..4>	Transmitter Non-Inverted Data Input
Rxn <1..4>	Receiver Inverted Data Output
Rxp <1..4>	Receiver Non-Inverted Data Output
SCL	2-Wire Serial Interface Clock
SDA	2-Wire Serial Interface Data
ModPrsL	Module Present
ModSelL	Module Select
ResetL	Module Reset
IntL	Interrupt
LPMode	Low Power Mode
Vcc Rx	+3.3 V Power Supply Receiver
Vcc Tx	+3.3 V Power Supply Transmitter
Vcc1	+3.3 V Power Supply
GND	Ground

Figure 3. CONNECTOR 0 and CONNECTOR 1

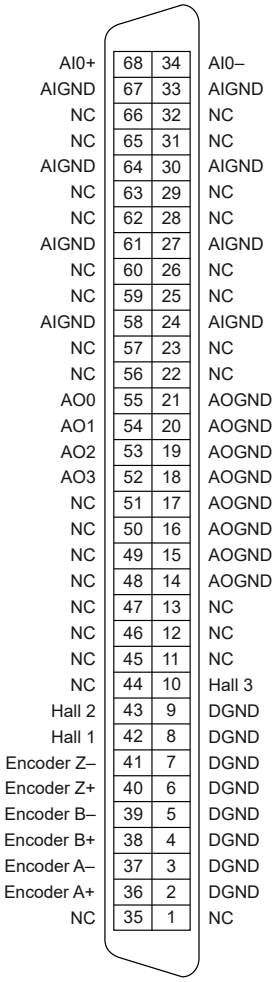


Table 3. Pin Descriptions for CONNECTOR 0 and CONNECTOR 1

Symbol	Description	Signal Name in LabVIEW
AI0+	Positive analog input	Conn0 AI0, Conn1 AI0
AI0-	Negative analog input	Conn0 AI0, Conn1 AI0
AIGND	Ground reference for analog input	—
AO <0..3>	Analog output	Conn0<AO 0..3>, Conn1<AO 0..3>
AOGND	Ground reference for analog output	—
Hall <1..3>	Hall Effect sensor output	Conn0 Hall<1..3>, Conn1 Hall<1..3>
Encoder <A/B/Z>±	Quadrature Encoder output	Conn0 EncoderA/B/Z, Conn1 EncoderA/B/Z

Symbol	Description	Signal Name in LabVIEW
DGND	Ground reference for the Hall Effect or Quadrature Encoder	—
NC	No connection	—

DIO

Connector	Molex™ Nano-Pitch I/O™
5.0 V power	±5%, 50 mA maximum

Table 4. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

MGT Tx± <0..3>

Data rate	500 Mb/s to 16.375 Gb/s, nominal
Number of Tx channels	4
I/O coupling	
Type	AC

Capacitor	100 nF
Minimum differential output voltage[1]	170 mV pk-pk into 100 Ω, nominal

Note For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

MGT Rx± <0..3>

Data rate	500 Mb/s to 16.375 Gb/s
Number of Rx channels	4
Differential input resistance	100 Ω
I/O coupling	
Type	DC
Capacitor	External capacitor required
Differential input voltage range	
≤6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
>6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal

1. When transmitter output swing is set to the maximum setting, the differential output voltage is 800 mV pk-pk.

Note For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

DIO <0..7>

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 5. DIO <0..7> Single-Ended DC Signal Characteristics[2]

Voltage Family	V_{IL}	V_{IH}	V_{OL}(100 µA Load)	V_{OH}(100 µA Load)	Maximum DC Drive Strength
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA

2. Voltage levels are guaranteed by design through the digital buffer specifications.

Voltage Family	V_{IL}	V_{IH}	V_{OL}(100 µA Load)	V_{OH}(100 µA Load)	Maximum DC Drive Strength
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA

PORT 0

Connector	QSFP+, SFF-8436 compliant
Data rate	5 Gb/s
Number of lanes	4 RX and 4 TX (GTH)
Supported high-speed cable type	Electrical, optical
Optical cable power	3.3 V ±5%, 1 A

CONNECTOR 0 and CONNECTOR 1

The following sections describe the input and output characteristics accessible through CONNECTOR 0 and CONNECTOR 1 on the PXIe-7899. CONNECTOR 0 and CONNECTOR 1 share the same pinout, which you can view in the ***PXIe-7899 Getting Started Guide*** at ni.com/manuals.

Connector	Dual stack 68-pin VHDCI receptacle

Note The number of channels listed in each of the following sections

> represents the total number of channels for both CONNECTOR 0 and CONNECTOR 1. To determine the number of channels for a single connector, divide the listed number of channels in half.

Analog Input

Input type	Differential
Number of channels	2
Signal names	Conn0 AI0, Conn1 AI0
Resolution	16 bits
Type of ADC	Successive approximation register (SAR)
Conversion latency	1µs
Analog latency	180 ns
Maximum sampling rate (per channel)	1 MS/s
Input impedance	
Powered on	1.25 GΩ ‖ 2 pF
Powered off/overload	4.32 kΩ

Input bias current	±5 nA
Input offset current	±5 nA
Input coupling	DC
INL	50 ppm maximum
DNL	±0.4 LSB typical, ±1.0 LSB maximum
CMRR, DC to 60 Hz	-80 dB
Bandwidth	
Small signal	
Ranges ±10 V, ±5 V, ±2 V	1.8 MHz
Range ±1 V	1.5 MHz
Large signal (1% THD)	
Range ±10 V	400 kHz
Ranges ±5 V, ±2 V, ±1 V	600 kHz
Crosstalk (100 kHz) into 50 Ω	-80 dB
Overvoltage protection	

Powered on	±42 V maximum
Powered off	±35 V maximum

Table 6. Analog Input Characteristics by Range

Specification	Nominal Range			
	±10 V	**±5 V**	**±2 V**	**±1 V**
Input Noise (µV RMS)	214	112	57	40
Gain Drift (ppm/°C)	±6.3	±6.3	±6.3	±6.3
Offset Drift (µV/°C)	±22	±11	±5	±3
Typical Input Range, AI+ to AI- (V)	±10.5	±5.25	±2.1	±1.05
Minimum[3] Input Range, AI+ to AI- (V)	±10.37	±5.18	±2.07	±1.03
Maximum Working Voltage (V) (signal + common mode to ground)	±12	±10	±8.5	±8

3. The minimum measurement voltage range is the largest voltage the PXIe-7899 is guaranteed to accurately measure.

Table 7. Analog Input Calibrated Accuracy

The following table shows the two-year warranted accuracy following a calibration performed at 25 °C, ±5 °C.

Nominal Range (V)	Conditions	Percent of Reading (Gain Error[6])	Percent of Range (Offset Error[4][4])
±10	Typical (25 °C, ±5 °C)	±0.00172%	±0.00558%
	Maximum (0 °C to 55 °C)	±0.0706%	±0.0138%
±5	Typical (25 °C, ±5 °C)	±0.00174%	±0.00598%
	Maximum (0 °C to 55 °C)	±0.0717%	±0.0141%
±2	Typical (25 °C, ±5 °C)	±0.00179%	±0.00650%
	Maximum (0 °C to 55 °C)	±0.0720%	±0.0142%
±1	Typical (25 °C, ±5 °C)	±0.00194%	±0.00643%
	Maximum (0 °C to 55 °C)	±0.0725%	±0.0147%

Table 8. Analog Input Uncalibrated Accuracy[5]

Nominal Range (V)	Conditions	Percent of Reading (Gain Error[6][6])	Percent of Range (Offset Error[4])
±10	Typical (25 °C, ±5 °C)	±0.089%	±0.027%
	Maximum (0 °C to 55 °C)	±0.33%	±0.13%
±5	Typical (25 °C, ±5 °C)	±0.090%	±0.028%
	Maximum (0 °C to 55 °C)	±0.34%	±0.14%
±2	Typical (25 °C, ±5 °C)	±0.090%	±0.029%

4. For offset error calculations, use the Typical Input Range value given in the ***Analog Input Characteristics by Range*** table. For example, use a value of 10.5 V for the ±10 V nominal range.
5. Uncalibrated accuracy refers to the accuracy achieved when acquiring data in raw or unscaled modes: when the calibration constants stored in the module are not applied to the data.
6. The gain error is relative to the Typical Input Range from the ***Analog Input Characteristics by Range*** table. For example, on the ±10 V nominal range, the gain error is relative to a full-scale value of 10.5 V.

Nominal Range (V)	Conditions	Percent of Reading (Gain Error[6])	Percent of Range (Offset Error[4])
	Maximum (0 °C to 55 °C)	±0.34%	±0.17%
±1	Typical (25 °C, ±5 °C)	±0.090%	±0.030%
	Maximum (0 °C to 55 °C)	±0.34%	±0.15%

Analog Output

Output type	Single-ended, voltage output
Number of channels	8
Signal names	Conn0 AO<0..3>, Conn1 AO<0..3>
Resolution	16 bits
Update latency	500 ns
Analog latency	185 ns
Maximum update rate	2 MS/s
Type of DAC	Enhanced R-2R
DNL	±0.5 LSB typical, ±1 LSB maximum

Output voltage range	
Nominal	±10 V
Typical	±10.12 V
Minimum	±10.1 V
Output coupling	DC
Gain drift	1.4 ppm/°C
Offset drift	6.9 uV/°C
Slew rate	20 V/µs
Noise	250 µV RMS, DC to 1 MHz
Glitch energy at midscale transition	±10 mV for 3 µs
Current drive	±15 mA
Protection	Short circuit to ground
Overvoltage protection	
Powered on	±15 V maximum

Powered off	±10 V maximum
Power-on glitch	300 mV for 70 ms
Power-off glitch	1.5 V for 200 µs
Glitch during FPGA loading	150 mV for 40 µs

Table 9. Analog Output Calibrated Accuracy

The following table shows the two-year warranted accuracy following a calibration performed at 25°C, ±5°C.

Nominal Range (V)	Conditions	Percent of Reading (Gain Error[])	Percent of Range[7] (Offset Error[])
±10	Typical (25 °C, ±5 °C)	±0.011%	±0.0091%
	Maximum (0 °C to 55 °C)	±0.041%	±0.028%

Table 10. Analog Output Uncalibrated Accuracy

Nominal Range (V)	Conditions	Percent of Reading (Gain Error[])	Percent of Range[7][7] (Offset Error[])
±10	Typical (25 °C, ±5 °C)	±0.061%	±0.034%
	Maximum (0 °C to 55 °C)	±0.145%	±0.028%

Hall Effect Digital Output

Note Because the Hall Effect and Quadrature Encoder Digital Outputs share the same internal resource, only one of the digital outputs can be used at a time.

7. Range equals 10.12 V.

Output type	Sinking (open drain) digital output
Number of channels	6
Signal names	Conn0 Hall<1..3>, Conn1 Hall<1..3>
Power-on state	Channels off
Output voltage (V_o)	I_o * R_o
Continuous sink current (I_o)	0.1 A per channel, maximum (from external pullup)
Output impedance (R_o)	0.065 Ω
Reversed voltage protection	None
Short circuit protection	None
External applied voltage range	0 V DC to 30 V DC
Update latency	100 ns
Transition time	Pullup value and cable dependent
Output capacitance	800 pF at 0 V, 300 pF at 5 V

Maximum recommended update rate	125 kHz

Quadrature Encoder Digital Output

Note Because the Hall Effect and Quadrature Encoder Digital Outputs share the same internal resource, only one of the digital outputs can be used at a time.

Output type	ISL3295E differential digital output
Number of channels	6 differential
Signal names	Conn0 EncoderA/B/Z, Conn1 EncoderA/B/Z
Voltage output differential	
at 100 Ω	2.3 V typical, 2 V minimum
at 54 Ω	2 V typical, 1.5 V minimum
no load	3.3 V typical
Update latency	100 ns
ESD protection	±16.5k V Human Body Model ±7k V IEC 61000-4-2 Contact Method

Output protection	Short circuit protection[8]

Calibration

Interval	2 years

Reconfigurable FPGA

FPGA	KU060
LUTs	331,680
DSP48 slices (25 × 18 multiplier)	2,760
Embedded Block RAM	38.0 Mb
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)
Data transfers	DMA, interrupts, programmed I/O, MGTs
Number of DMA channels	60

Note The list above depicts the total number of FPGA resources available on

8. The short circuit protection utilizes current foldback. In extreme cases, the protection triggers a thermal shutdown. To re-enable the output after a shutdown, remove the short. After the short is removed, it may take up to twenty seconds for the output to return to an operable state.

the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI Technical Support at ni.com/support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	4.0 cm × 13.0 cm × 21.6 cm(1.57 in. × 5.12 in. × 8.50 in.)
Weight	680 g (23.99 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[9]

9. The PXIe-7899 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the PXI Chassis Manual for specifications to determine the ambient temperature ranges your chassis can achieve.

Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing