PCI-6542 Specifications

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Contents

PCI-6542 Specifications

These specifications apply to the PCI-6542 with 1 MBit, 8 MBit, and 64 MBit of memory per channel.

> **Note** All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are ***Typical*** unless otherwise noted.

Conditions

Typical values are representative of an average unit operating at room temperature.

PCI-6542 Pinout

Use the pinout to connect to terminals on NI 654x devices.

Figure 1. NI 654x Connector Pinout

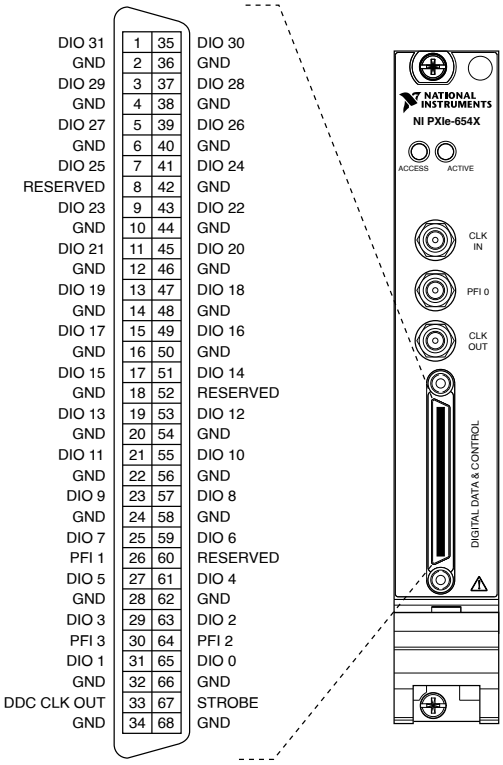


Table 1. NI 654x DDC Connector Pins

Pins	Signal Name	Signal Type	Signal Description
33	DDC_CLK OUT	Control	Output terminal for the exported Sample Clock.
67	Strobe	Control	Terminal for the external Sample clock source, which can be used for dynamic acquisition.
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65	DIO <0..31>	Data	Bidirectional digital I/O data channels 0 through 31.
26, 30, 64	Programmable Function Interface (PFI) <1..3>	Control	Input terminals to the device for external triggers, or output terminals from the device for events.
2, 4, 6, 10, 12, 14, 16, 18, 20, 22, 24, 28, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 54, 56, 58,	GND	Ground	Ground reference for signals.

Pins	Signal Name	Signal Type	Signal Description
62, 66			
8, 52, 60	RESERVED	N/A	Terminals reserved for future use. Do not connect to these pins.

Channels

Data	
Number of channels	32
Direction control	Per channel
Programmable Function Interface (PFI)	
Number of channels	4
Direction control	Per channel
Clock terminals	
Input	3
Output	2

Generation Channels

Channels	Data DDC CLK OUT

	PFI <0..3>
Signal type	Single-ended

Table 2. Voltage Levels, I = 100 µA

Logic family, into 1 MΩ	Low		High	
	Typical	Maximum	Minimum	Typical
1.8 V	0 V	0.1 V	1.7 V	1.8 V
2.5 V			2.4 V	2.5 V
3.3 V TTL (5 V TTL compatible)			3.2 V	3.3 V

Output impedance	50 Ω, nominal
Maximum DC drive strength, by logic family	
1.8 V	±8 mA
2.5 V	±16 mA
3.3 V	±32 mA
Data channel driver enable/disable control	Software-selectable: per channel
Channel power-on state[1]	Drivers disabled, 50 kΩ input impedance
Output protection	

1. For module assemblies C and later. Module assemblies A and B have an input impedance of 10 kΩ.

Range	0 V to 5 V
Duration	Indefinite

Acquisition Channels

Channels	Data STROBE PFI <0..3>
Signal type	Single-ended

Table 3. Voltage Levels

Logic family	Maximum Low Threshold	Minimum High Threshold
1.8 V	0.45 V	1.35 V
2.5 V	0.75 V	1.75 V
3.3 V TTL (5 V TTL compatible)	1.00 V	2.30 V

Input impedance[2]	50 kΩ
Input protection range[3]	-1 V to 6 V

2. For module assemblies C and later. Module assemblies A and B have an input impedance of 10 kΩ.
3. Diode clamps in the design may provide additional protection outside the specified range.

Timing

Sample Clock

Sources	1. On Board clock (internal voltage-controlled crystal oscillator [VCXO] with divider) 2. CLK IN (SMB jack connector) 3. STROBE (Digital Data & Control [DDC] connector; acquisition only)
Frequency range	
On Board clock	48 Hz to 100 MHz, Configurable to 200 MHz/***N;*** $2 \leq N \leq 4{,}194{,}304$
CLK IN	20 kHz to 100 MHz
STROBE	48 MHz to 100 MHz
Relative delay adjustment[4]	
Range	0.0 to 1.0 Sample clock periods
Resolution	10 ps
Exported Sample clock	
Destinations[5]	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)

4. You can apply a delay or a phase adjustment to the On Board clock to align multiple devices.

Delay (δ_C), for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period
Jitter, using On Board clock	
Period	20 ps_{rms}, typical
Cycle-to-cycle	35 ps_{rms}, typical

Generation Timing

Channels	Data DDC CLK OUT PFI <0..3>
Data channel-to-channel skew	±600 ps, typical
Maximum data channel toggle rate	50 MHz
Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Generation data delay (δ_G), for clock frequencies ≥25 MHz	

5. Sample clocks with sources other than STROBE can be exported.

Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period
Exported Sample clock offset (t_{CO})	Software-selectable: 0.0 ns or 2.5 ns (default)
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	15 ns, typical

Table 4. Generation Provided Setup and Hold Times

Exported Sample Clock Mode and Offset	Voltage Family	Time from Rising Clock Edge to Data Transition (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
Noninverted, 2.5 ns	1.8 V	2.5 ns, typical	t_P - 5.5 ns	0.5 ns
	2.5 V		t_P - 4.5 ns	0.9 ns
	3.3 V/5.0 V		t_P - 4.5 ns	1 ns
Inverted, 0 ns	1.8 V	$t_P/2$	$t_P/2$ - 3.5 ns	($t_P/2$) - 1.5 ns
	2.5 V		$t_P/2$ - 2.5 ns	
	3.3 V/5.0 V		$t_P/2$ - 2 ns	

Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.

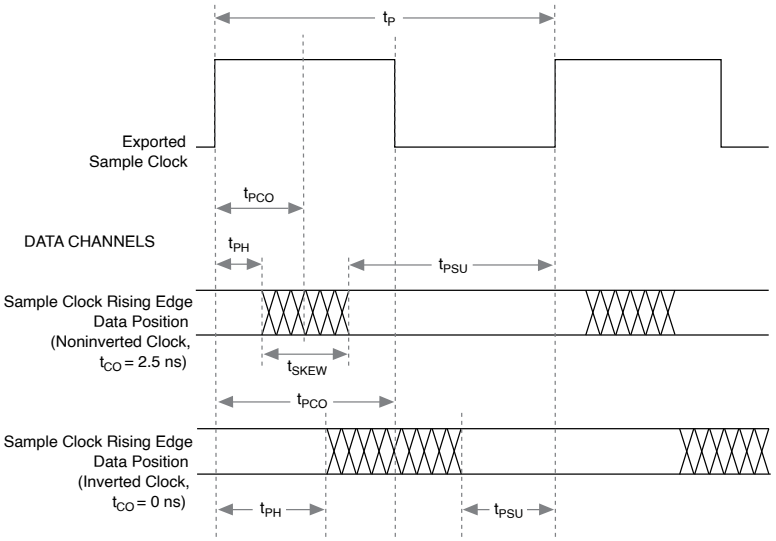
The table values provided assume the following data position is set to Sample clock rising edge and the Sample clock is exported to the DDC connector and includes worst-case effects of channel-to-channel skew, inter-symbol interference, and jitter. Other combinations of exported Sample clock mode and offset are also allowed. The values

presented are from the default case (noninverted clock with 2.5 s offset) and for providing balanced setup and hold times (inverted clock with 0 ns offset).

To determine the appropriate exported Sample clock mode and offset for your PCI-6542 generation session, compare the setup and hold times from the datasheet of your device under test (DUT) to the values in this table. Select the exported Sample clock mode and offset such that the PCI-6542 provided setup and hold times are greater than the setup and hold times required for the DUT.

Specified timing relationships apply at the DDC connector and at high-speed DIO accessory terminals. Any signal routing, clock splitting, buffers, or translation logic can impact this relationship. If multiple copies of DDC_CLK_OUT are necessary, use a zero buffer to preserve this relationship.

Figure 2. Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{f}$ = Sample Clock Period

t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Set-Up Time

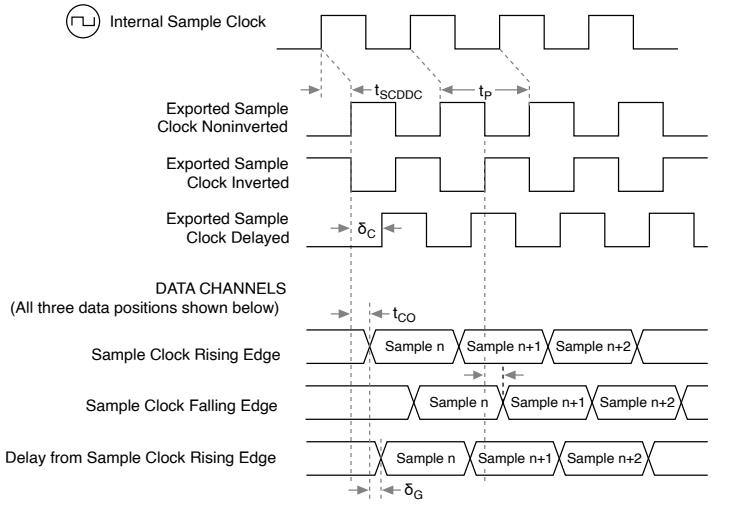
t_{PCO} = Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time

t_{CO} = Exported Sample Clock Offset

t_{SKEW} = Maximum Channel-to-Channel Skew and Clock Uncertainty

Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.

Figure 3. Generation Timing Diagram



t_{SCDDC} : Time Delay from Internal Sample Clock to DDC Connector Exported Sample Clock

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (fraction of t_P)

$0 \le \delta_G \le 1$: Generation Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

t_{CO} = Exported Sample Clock Offset; 0 or 2.5 ns, software-selectable

Acquisition Timing

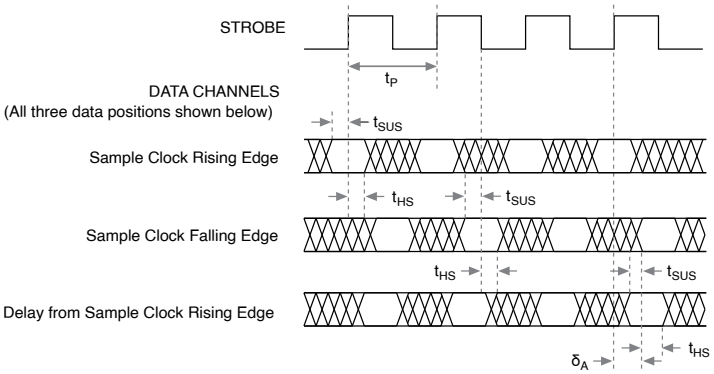
Channels	Data STROBE PFI <0..3>
Channel-to-channel skew	±600 ps, typical
Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Setup and hold times	
To STROBE[6]	

6. Includes maximum data channel-to-channel skew.

Setup time (t_{SUS})	3.1 ns, maximum
Hold time (t_{HS})	2.7 ns, maximum
To Sample clock[7]	
Setup time (t_{SUSC})	0.4 ns
Hold time (t_{HSC})	0 ns
Time delay from DDC connector data to internal Sample clock (t_{DDCSC})	10 ns, typical
Acquisition data delay (δ_A), for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period

7. Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}.

Figure 4. Acquisition Timing Diagram Using STROBE as the Sample Clock



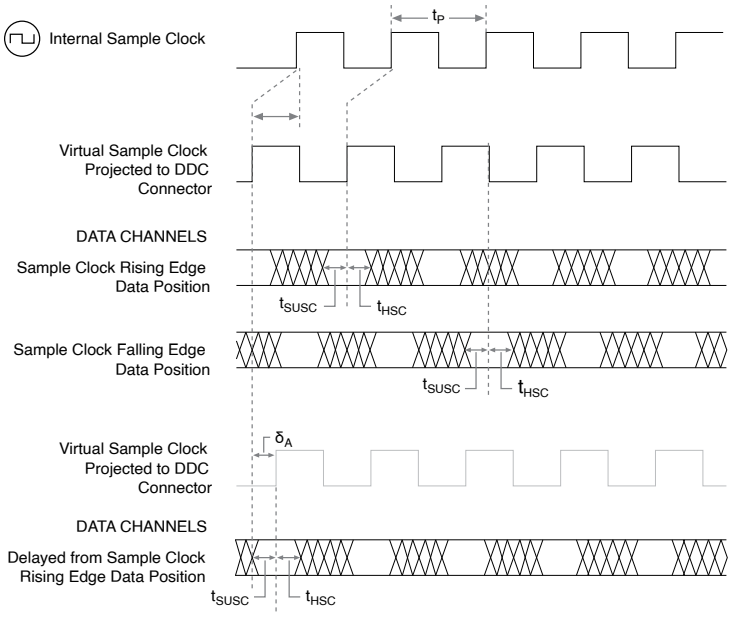
t_{SUS} = Set-Up Time to STROBE

t_{HS} = Hold Time from STROBE

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

Figure 5. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

CLK IN

Connector	SMB jack

Direction	Input
Signal type	Single-ended
Destinations	1. Reference clock for the phase-locked loop (PLL) 2. Sample clock
Input coupling	AC
Input protection	±10 VDC
Input impedance	Software-selectable: 50 Ω (default) or 1 kΩ
Minimum detectable pulse width	4 ns
Clock requirements	Free-running (continuous) clock

As Sample Clock

Table 5. External Sample Clock Range

Voltage Range (V_{pk-pk})	Sine Wave	Square Wave	
	Frequency Range	Frequency Range	Duty Cycle
0.65 to 5.0	5.5 MHz to 100 MHz	20 kHz to 100 MHz	• f <50 MHz: 25% to 75% • f ≥50 MHz: 40% to 60%

Voltage Range (V_{pk-pk})	Sine Wave	Square Wave	
	Frequency Range	Frequency Range	Duty Cycle
1.0 to 5.0	3.5 MHz to 100 MHz	—	—
2.0 to 5.0	1.8 MHz to 100 MHz	—	—

As Reference Clock

Frequency range	10 MHz ±50 ppm
Voltage range	0.65 V_{pk-pk} to 5.0 V_{pk-pk}
Duty cycle	25% to 75%

STROBE

Connector	DDC
Direction	Input
Destination	Sample clock (acquisition only)
Frequency range	48 MHz to 100 MHz
Duty cycle range[8]	
f <50 MHz	25% to 75%

8. At the programmed thresholds.

f ≥50 MHz	40% to 60%
Minimum detectable pulse width[9]	4 ns
Voltage thresholds	Refer to Acquisition Timing in the ***Timing*** section.
Clock requirements	Free-running (continuous) clock
Input impedance[10]	Software-selectable: 50 kΩ

CLK OUT

Connector	SMB jack
Direction	Output
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)
Output impedance	50 Ω, nominal
Electrical characteristics	Refer to Generation Timing in the ***Timing*** section.
Maximum drive current	

9. Required at both acquisition voltage thresholds.
10. For module assemblies C and later. Module assemblies A and B have an input impedance of 10 kΩ.

At 1.8 V	8 mA
At 2.5 V	16 mA
At 3.3 V	32 mA
Logic type	Generation logic family setting: 1.8 V, 2.5 V, 3.3 V

DDC CLK OUT

Connector	DDC
Direction	Output
Source[11]	Sample clock
Electrical characteristics	Refer to Generation Timing in the ***Timing*** section.

Reference Clock (PLL)

Sources[12]	1. RTSI 7 2. CLK IN (SMB jack connector) 3. None (On Board clock not locked to a reference)

11. STROBE cannot be routed to DDC CLK OUT.
12. The source provides the reference frequency for the PLL.

Destination	CLK OUT (SMB jack connector)
Lock time	400 ms, typical
Frequencies	10 MHz ±50 ppm
Duty cycle range	25% to 75%

Waveform

Memory and Scripting

Memory architecture	The PCI-6542 uses Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user defined.
Onboard memory size[13]	
1 Mbit/channel	
Acquisition	1 Mbit/channel (4 MBytes total)
Generation	1 Mbit/channel (4 MBytes total)
8 Mbit/channel	
Acquisition	8 Mbit/channel (32 MBytes total)

13. Maximum limit for generation sessions assumes no scripting instructions.

Generation	8 Mbit/channel (32 MBytes total)
64 Mbit/channel	
Acquisition	64 Mbit/channel (256 MBytes total)
Generation	64 Mbit/channel (256 MBytes total)
Generation	
Single waveform mode	Generates a single waveform once, ***n*** times, or continuously.
Scripted mode[14]	Generates a simple or complex sequence of waveforms.
Finite repeat count	1 to 16,777,216
Waveform quantum	Waveform must be an integer multiple of 2 S (samples).[15]

Table 6. Generation Minimum Waveform Size, Samples (S)[16]

Configuration	Sample Rate	
	100 MHz	50 MHz
Single waveform	2 S	2 S
Continuous waveform	32 S	16 S
Stepped sequence	128 S	64 S

14. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.
15. Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.
16. Sample rate dependent. Increasing sample rate increases minimum waveform size.

Configuration	Sample Rate	
	100 MHz	50 MHz
Burst sequence	512 S	256 S

Acquisition	
Minimum record size[17]	1 S
Record quantum	1 record
Total records	2,147,483,647, maximum
Total pre-Reference trigger samples	0 up to full record
Total post-Reference trigger samples	0 up to full record

Triggers

Trigger Types	Sessions	Edge Detection	Level Detection
1. Start	Acquisition and generation	Rising or Falling	—
2. Pause	Acquisition and generation	—	High or Low
3. Script <0..3>	Generation	Rising or Falling	High or Low
4. Reference	Acquisition	Rising or Falling	—
5. Advance	Acquisition	Rising or Falling	—

Sources	1. PFI 0 (SMB jack connector)

17. Regardless of waveform size, NI-HSDIO allocates at least 128 bytes for a record.

	2. PFI <1..3> (DDC connector) 3. RTSI <0..7> (RTSI bus) 4. Pattern match (acquisition sessions only) 5. Software (user function call) 6. Disabled (do not wait for a trigger)
Destinations[18]	PFI 0 (SMB jack connector) PFI <1..3> (DDC connector) RTSI <0..6> (RTSI bus)
Minimum required trigger pulse width	
Generation	30 ns
Acquisition	Acquisition triggers must meet setup and hold time requirements.

Table 7. Trigger Rearm Time

Trigger Operation	Samples, Typical	Samples, Maximum
Start to Reference	57 S	64 S
Start to Advance	138 S	143 S
Reference to Reference	132 S	153 S

Delay from Pause trigger to Pause state[19]	
Generation sessions	32 Sample clock periods + 150 ns

18. Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.

Acquisition sessions	Data synchronous
Delay from trigger to digital data output	32 Sample clock periods + 160 ns

Events

Event Types	Sessions
1. Marker <0..3>	Generation
2. Data Active	Generation
3. Ready for Start	Acquisition and generation
4. Ready for Advance	Acquisition
5. End of Record	Acquisition

Destinations[20]	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. RTSI <0..6> (RTSI bus)
Marker time resolution (placement)	Markers must be placed at an integer multiple of 2 S (samples).

Miscellaneous

Warm-up time	15 minutes

19. Use the Data Active event during generation to determine when the PCI-6542 enters the Pause state.
20. Except for the Data Active event, each event can be routed to any destination. The Data Active event can be routed only to the PFI channels.

On Board clock characteristics (valid only when PLL reference source is set to None)	
Frequency accuracy	±100 ppm
Temperature stability	±30 ppm
Aging	±5 ppm first year

Power

VDC	Current Draw, Typical	Current Draw, Maximum
+3.3 V	1.6 A	1.8 A
+5 V	1.2 A	1.7 A
+12 V	0.25 A	0.4 A
-12 V	0.06 A	0.10 A

Total power	15 W, typical 20.5 W, maximum

Physical Specifications

Dimensions	12.6 cm × 35.5 cm
Weight	410 g (14.5 oz)

I/O Connectors

Label	Connector Type	Description
CLK IN	SMB jack	External Sample clock, external PLL reference input
PFI 0		Events, triggers
CLK OUT		Exported Sample clock, exported Reference clock
DIGITAL DATA & CONTROL	68-pin VHDCI connector	Digital data channels, exported Sample clock, STROBE, events, triggers

Software

Driver Software

Driver support for this device was first available in NI-HSDIO 1.2.

NI-HSDIO is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-6542. NI-HSDIO provides application programming interfaces for many development environments.

Application Software

NI-HSDIO provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

NI Measurement Automation Explorer

NI Measurement Automation Explorer (MAX) provides interactive configuration and test tools for the PCI-6542. MAX is included on the NI-HSDIO media.

Environment

Note To ensure that the PCI-6542 cools effectively, follow the guidelines in the ***Maintain Forced Air Cooling Note to Users*** included with the PCI-6542 or available at ni.com/manuals. The PCI-6542 is intended for indoor use only.

Operating temperature	0 °C to 45 °C
Operating relative humidity	10 to 90% relative humidity, noncondensing (meets IEC 60068-2-56)
Storage temperature	-20 °C to 70 °C (meets IEC 60068-2-2)
Storage relative humidity	5 to 95% relative humidity, noncondensing (meets IEC 60068-2-56)
Altitude	0 to 2,000 m above sea level (at 25 °C ambient temperature)
Pollution degree	2

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations, certifications, and additional information, refer to the Online Product Certification section.

To meet EMC compliance, the following cautions apply:

Caution The SHC68-C68-D4 shielded cables must be used when operating the PCI-6542.

Caution EMC filler panels must be installed in all empty chassis slots.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)