PXIe-5171 Specifications

2025-03-10

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. ***Warranted*** specifications account for measurement uncertainties, temperature drift, and aging. ***Warranted*** specifications are ensured by design, or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured (meas)*** specifications describe the measured performance of a representative model.

Specifications are ***Nominal*** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- Sample rate set to 250 MS/s
- Onboard sample clock locked to onboard reference clock
- PXIe-5171 module warmed up for 15 minutes at ambient temperature.[1]
- PXI Express chassis fan speed set to HIGH, foam fan filters removed if present, and empty slots contain PXI chassis slot blockers and filler panels. For more

1. Warm-up begins after the chassis is powered, the device is recognized by the host, and the ADC clock is configured using either instrument design libraries or the NI-SCOPE device driver.

information about cooling, refer to the ***Maintain Forced-Air Cooling Note to Users*** available at ni.com/docs.
- Calibration IP used properly when using LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries) to create FPGA bitfiles. Refer to the ***NI Reconfigurable Oscilloscopes Help*** for more information about the calibration API.

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 45 °C
- External calibration cycle maintained
- External calibration performed at 23 °C ± 3 °C

Typical specifications are valid under the following conditions unless otherwise noted.

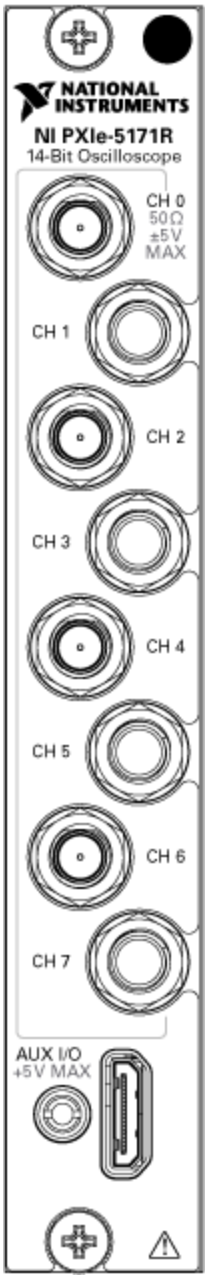
- Ambient temperature ranges of 0 °C to 45 °C

Nominal and Measured specifications are valid under the following conditions unless otherwise noted.

- Room temperature, approximately 23 °C

PXIe-5171 Front Panel

This section describes the front panel and connectors of the PXIe-5171.



Front Panel Connectors

Label	Connector Type	Function
CH 0—CH 7	SMA connector	Analog input terminal
AUX I/O	MHDMR connector	Sample Clock or Reference Clock input, Reference Clock output, bidirectional digital PFI, and 3.3 V power output

Label	Connector Type	Function
		Note This connector is referred to as AUX 0 in this document.

Note The AUX 0 connector accepts a standard, third-party HDMI™ type C cable, but the AUX 0 port is not an HDMI interface and the specified performance of the AUX 0 connector is not guaranteed if a third-party HDMI cable is used. Use NI cable type SHH19-MH19-AUX for all AUX 0 connections. Do not connect the AUX 0 port on the PXIe-5171 to the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.

PXIe-5171 Pinout

Use the pinout to connect to terminals on the PXIe-5171.

Figure 1. PXIe-5171 AUX 0 Connector Pinout

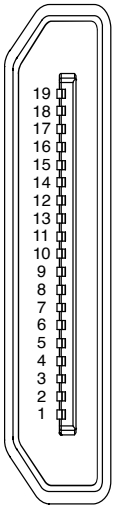


Table 1. AUX 0 Connector Pin Assignments

Pin	Signal	Signal Description
1	GND	Ground reference for signals
2	CLK IN	Used to import an external Reference Clock or Sample Clock

Pin	Signal	Signal Description
3	GND	Ground reference for signals
4	GND	Ground reference for signals
5	CLK OUT	Used to export the Reference Clock
6	GND	Ground reference for signals
7	GND	Ground reference for signals
8	AUX 0/PFI 0	Bidirectional PFI line
9	AUX 0/PFI 1	Bidirectional PFI line
10	GND	Ground reference for signals
11	AUX 0/PFI 2	Bidirectional PFI line
12	AUX 0/PFI 3	Bidirectional PFI line
13	GND	Ground reference for signals
14	AUX 0/PFI 4	Bidirectional PFI line
15	AUX 0/PFI 5	Bidirectional PFI line
16	AUX 0/PFI 6	Bidirectional PFI line
17	AUX 0/PFI 7	Bidirectional PFI line
18	+3.3 V	+3.3 V power (200 mA maximum)
19	GND	Ground reference for signals

PXIe-5171 SCB-19 Pinout

You can use the SCB-19 connector block to connect digital signals to the AUX 0 connector on the PXIe-5171 front panel. Refer to the following figure and table for information about the SCB-19 signals when connected to the AUX 0 front panel connector.

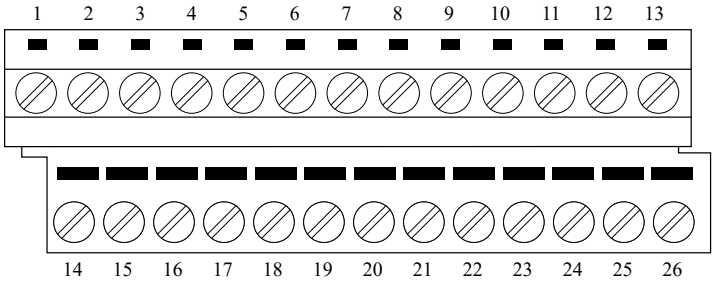


Table 2. SCB-19 Signal Descriptions

Pin	Signal	Signal Description
1	PFI 0	Bidirectional PFI line
2	PFI 1	Bidirectional PFI line
3	PFI 2	Bidirectional PFI line
4	PFI 3	Bidirectional PFI line
5	NC	No connection
6	CLK IN	Used to import an external reference clock or sample clock
7	NC	No connection
8	CLK OUT	Used to export the reference clock
9	PFI 4	Bidirectional PFI line
10	PFI 5	Bidirectional PFI line
11	PFI 6	Bidirectional PFI line
12	PFI 7	Bidirectional PFI line
13	+3.3 V	+3.3 V power (200 mA maximum)
14 to 26	GND	Ground reference for signals

PXIe-5171 AUX 0 Breakout Cable to 6 BNCs Pinout

You can use the AUX 0 Breakout Cable to 6 BNCs to connect digital signals to the AUX 0 connector on the PXIe-5171 front panel. Refer to the following figure and table for information about the AUX 0 Breakout Cable to 6 BNCs signals when connected to the

AUX 0 front panel connector.

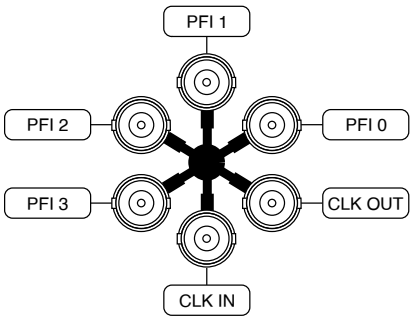


Table 3. AUX 0 Breakout Cable to 6 BNCs Signal Descriptions

Signal	Connector Type	Description
CLK IN	BNC female	Used to import an external reference clock
CLK OUT		Used to export the reference clock
PFI 0		Bidirectional PFI line
PFI 1		Bidirectional PFI line
PFI 2		Bidirectional PFI line
PFI 3		Bidirectional PFI line

Vertical

Analog Input

Number of channels	8 (simultaneously sampled)
Input type	Referenced single-ended
Connectors	SMA

Impedance and Coupling

Input impedance	50 Ω ± 1.5%, typical
Input coupling	AC, DC

Figure 1. Voltage Standing Wave Ratio (VSWR)

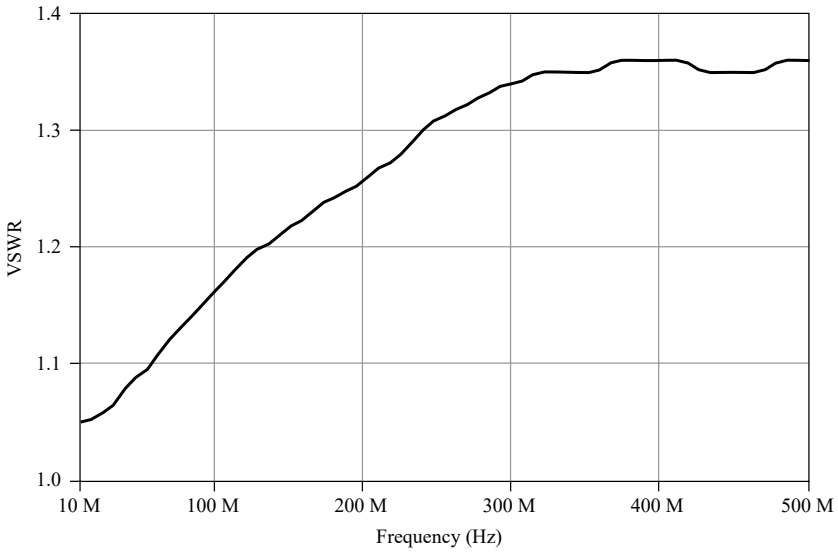
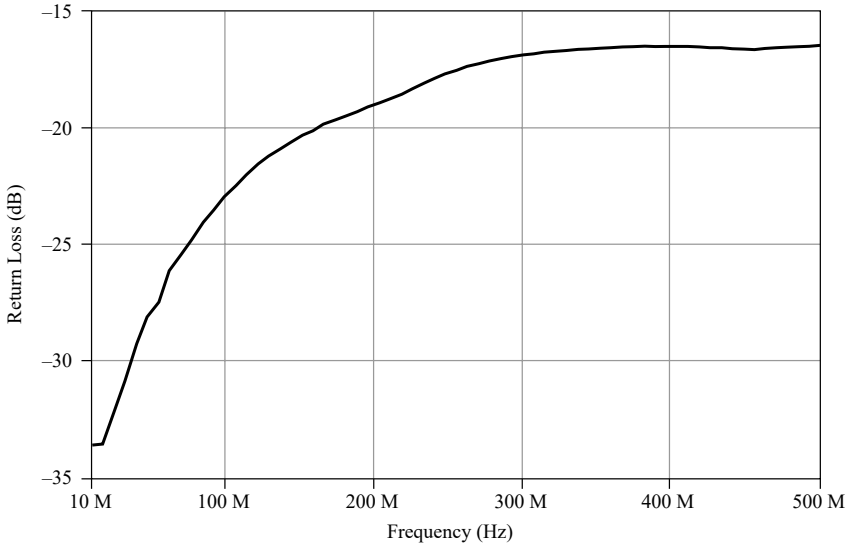


Figure 1. Input Return Loss



Voltage Levels

Full-scale (FS) input range (V_{pk-pk})	0.2 V 0.4 V 1 V 2 V 5 V
Maximum input overload[2]	|Peaks| ≤ 5 V

Accuracy

Notice Electromagnetic interference can adversely affect the measurement accuracy of this product. The coaxial channel inputs of this device (CH 0 to CH 7) are not protected for electromagnetic interference. As a result, this device may experience reduced measurement accuracy or other temporary performance degradation when connected cables are routed in an environment with radiated or conducted radio frequency electromagnetic interference. To limit radiated emissions and to ensure that this device functions within specifications in its operational electromagnetic environment, take precautions when designing, selecting, and installing measurement probes and cables.

Resolution	14 bits

2. Signals exceeding the maximum input overload may cause damage to the device.

Table 4. DC Accuracy[3]

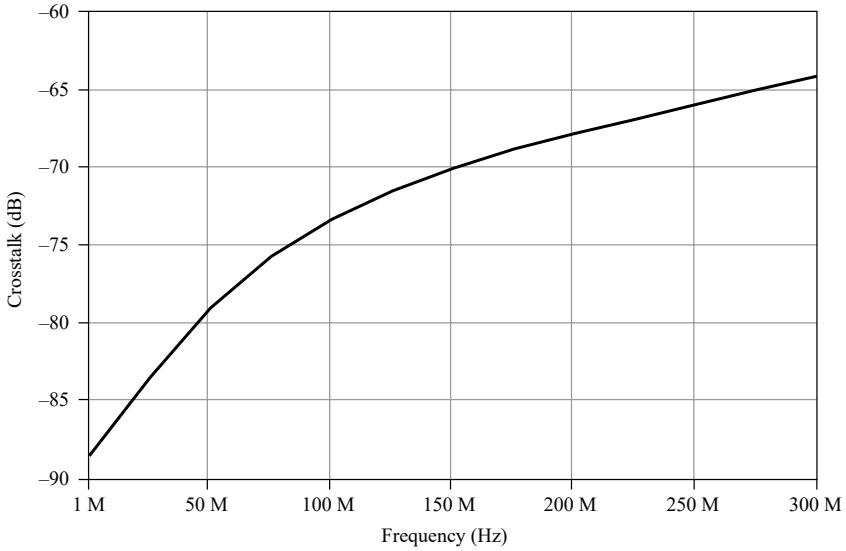
Input Range	Accuracy		Drift
	Typical[4]	Warranted[5]	Nominal[6]
V_{pk-pk}	±(% of |Reading|+ % of FS+ mV)	±(% of |Reading|+ % of FS+ mV)	±(% of |Reading|+ % of FS+ mV) per °C
0.2 V	±(0.45 + 0.6 + 0.2)[34]	±(0.90 + 0.65 + 0.7) [5]	±(0.015 + 0.002 + 0.004) [6]
0.4 V	±(0.45 + 0.24 + 0.2)	±(0.80 + 0.25 + 0.7)	±(0.012 + 0.002 + 0.004)
1 V	±(0.45 + 0.2 + 0.2)	±(0.80 + 0.25 + 0.7)	±(0.010 + 0.002 + 0.004)
2 V	±(0.40 + 0.2 + 0.2)	±(0.60 + 0.25 + 0.7)	±(0.005 + 0.002 + 0.004)
5 V	±(0.40 + 0.2 + 0.2)	±(0.55 + 0.25 + 0.7)	±(0.005 + 0.002 + 0.004)

DC accuracy sampling drift, full bandwidth (±% of |Reading| per MHz from 250 MHz)[7] $\frac{250MHz - frequency}{1,000,000} \times DCaccuracysamplingdrift$	±0.03, nominal
AC amplitude accuracy[3]	
Accuracy	±0.095 dB at 50 kHz, typical[4]

3. Verification of these specifications requires the ***DC Adjustment Device Temperature (°C)*** value. If you are using version 14.0 of the software, visit ni.com/info and enter the Info Code exxpmp for information on how to read this value. Otherwise, use NI-SCOPE to read the value.
4. When the reading from the ***Device Temperature*** sensor is within ±10 °C of the ***DC Adjustment Device Temperature (°C)*** value.
5. When the reading from the ***Device Temperature*** sensor is within ±38 °C of the ***DC Adjustment Device Temperature (°C)*** value. This increased temperature span encompasses the majority of temperature differences between the last external calibration environment and the operating environment.
6. Used to calculate additional temperature error when the difference between the ***Device Temperature*** sensor and the ***DC Adjustment Device Temperature (°C)*** value is greater than ±10 °C (for typical specifications) or ±38 °C (for warranted specifications).
7. Used to calculate additional DC accuracy error when using an external sample clock of frequency <250 MHz. To calculate the additional error, solve the following for the analog path of interest:

	±0.15 dB at 50 kHz, warranted[5]
Drift[6]	±0.0013 dB per °C
Conversion error rate[8]	
250 MS/sec	$<1 \times 10^{-10}$
200 MS/sec	$<1 \times 10^{-15}$
150 MS/sec	$<1 \times 10^{-20}$

Figure 1. Channel-to-Channel Crosstalk[9]



8. A ***conversion error*** is defined as deviation greater than 0.6% of full scale.
9. Measured on one channel with test signal applied to another channel, with the same range setting on both channels.

Bandwidth and Transient Response

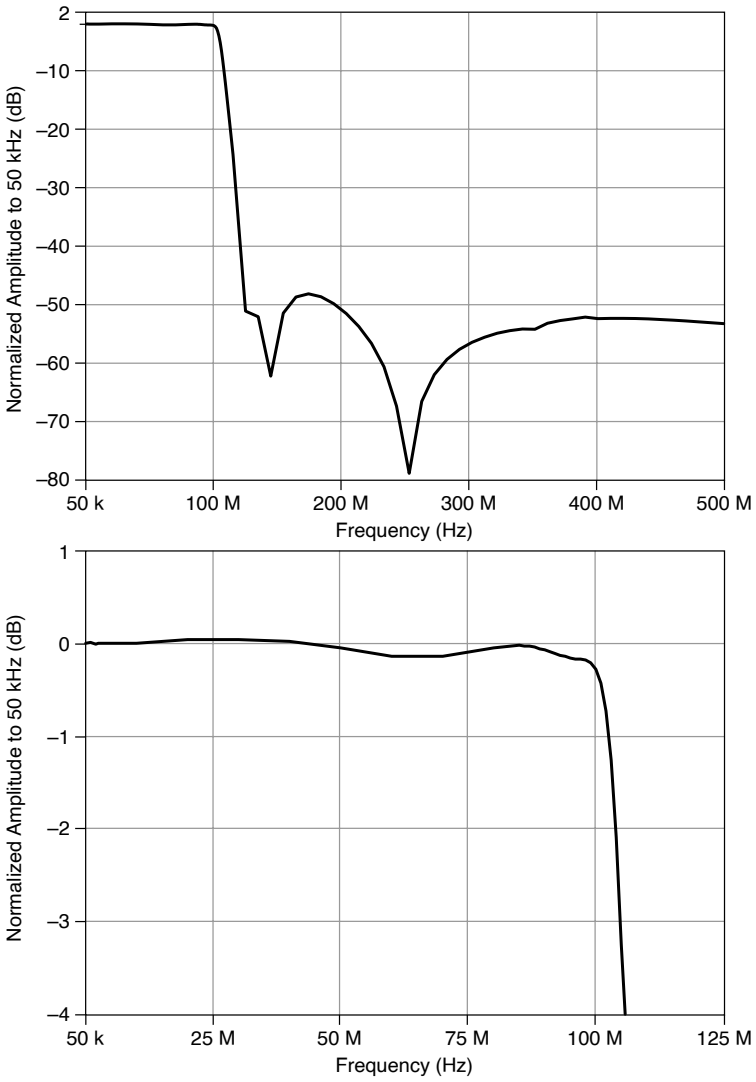
Bandwidth-limiting filter	100 MHz anti-alias filter
Bandwidth (-3 dB)GUID-18EAD082-4C17-40EC-9D69-1193909CD1BE.html#GUID-18EAD082-4C17-40EC-9D69-1193909CD1	
Anti-alias filter	
Full bandwidth	
0.2 V_{pk-pk} input range	260 MHz
All other input ranges	270 MHz

Table 5. Passband Amplitude Flatness, Warranted[10]10

Input Frequency	Anti-Alias Filter Enabled	Full Bandwidth
<50 MHz	-0.5 dB to 0.5 dB	-0.5 dB to 0.5 dB
≥50 MHz to <90 MHz	-1.0 dB to 0.5 dB	-0.75 dB to 0.5 dB
≥90 MHz to <100 MHz	—	-0.75 dB to 0.5 dB
≥100 MHz to <150 MHz	—	-1 dB to 0.5 dB

AC-coupling cutoff (-3 dB)[11]	120 kHz

10. Normalized to 50 kHz.
11. With AC coupling enabled, the input impedance is 260 kΩ to ground. Verified using a 50 Ω source.



Spectral Characteristics

Table 6. Spurious-Free Dynamic Range (SFDR)[12]12

Input Range (V_{pk-pk})	Input Frequency	Full Bandwidth
0.2 V to 2 V	<10 MHz	-80.0 dBc
	≥10 MHz to <30 MHz	-76.0 dBc
5 V	<10 MHz	-77.0 dBc
	≥10 MHz to <30 MHz	-73.0 dBc

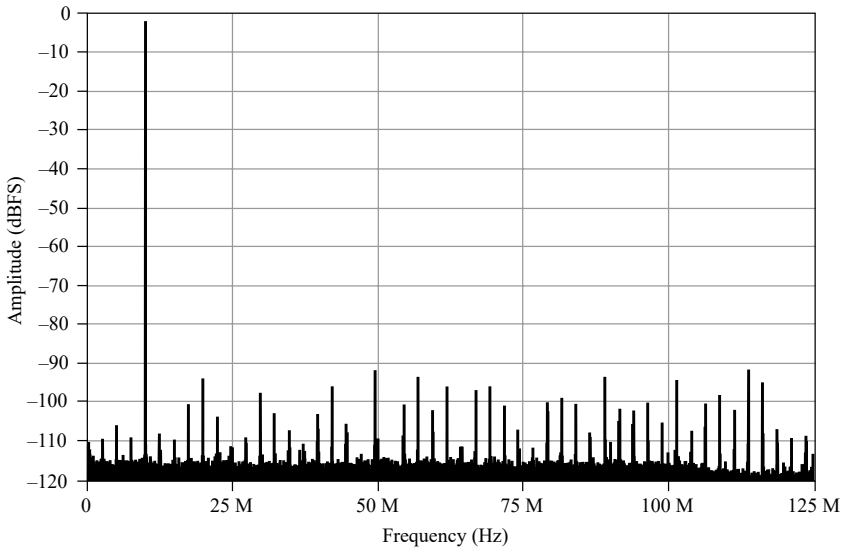
12. -1 dBFS input signal corrected to FS. 358 Hz resolution bandwidth (RBW).

Table 7. Total Harmonic Distortion (THD)[13]

Input Frequency	Full Bandwidth
<10 MHz	-77.0
≥10 MHz to <30 MHz	-73.0

Table 8. Effective Number of Bits (ENOB)[12]

Input Range (V_{pk-pk})	Input Frequency	Full Bandwidth
0.2 V	<30 MHz	10.8
All other input ranges	<30 MHz	11.0



Noise

RMS noise[GUID-204DFAF7-77C3-4329-B5A1-BDEA7EF6BB2A.html#GUID-204DFAF7-77C3-4329-B5A1-BDEA7EF6BB](GUID-204DFAF7-77C3-4329-B5A1-BDEA7EF6BB2A.html#GUID-204DFAF7-77C3-4329-B5A1-BDEA7EF6BB)	
Anti-alias filter enabled	0.017% of FS, typical
Full bandwidth	
0.2 V_{pk-pk} input range	0.037% of FS, typical

13. Includes the second through the fifth harmonics. -1 dBFS input signal.

0.4 V_{pk-pk} input range	0.025% of FS, typical
All other input ranges	0.024% of FS, typical

Table 9. Average Noise Density (dBm/Hz), Typical[14]14

Input Range (V_{pk-pk})	Anti-Alias Filter Enabled (dBm/Hz)	Full Bandwidth (dBm/Hz)
0.2 V	-159.2 dBm/Hz	-153.6 dBm/Hz
0.4 V	-153.7 dBm/Hz	-150.4 dBm/Hz
1 V	-145.7 dBm/Hz	-142.4 dBm/Hz
2 V	-139.7 dBm/Hz	-136.4 dBm/Hz
5 V	-131.7 dBm/Hz	-128.4 dBm/Hz

Table 10. Average Noise Density (dBFS/Hz), Typical[14]

Input Range (V_{pk-pk})	Anti-Alias Filter Enabled (dBFS/Hz)	Full Bandwidth (dBFS/Hz)
0.2 V	149.2 dBFS/Hz	143.6 dBFS/Hz
All other input ranges	149.7 dBFS/Hz	146.4 dBFS/Hz

Table 11. Average Noise Density (nV/√Hz), Typical[14]

Input Range (V_{pk-pk})	Anti-Alias Filter Enabled (nV/√Hz)	Full Bandwidth (nV/√Hz)
0.2 V	3.5 nV/√Hz	6.6 nV/√Hz
0.4 V	6.5 nV/√Hz	9.6 nV/√Hz
1 V	16.4 nV/√Hz	23.9 nV/√Hz
2 V	32.7 nV/√Hz	47.9 nV/√Hz
5 V	81.8 nV/√Hz	119.7 nV/√Hz

14. Verified using a 50 Ω terminator connected to input.

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCXO)
External	AUX I/O CLK IN (front panel MHDMR connector) PXIe_DStarA (backplane connector)

Sample rate range, real-time[15]	3.815 kS/s to 250 MS/s
Timebase frequency	
Internal	250 MHz
External	150 MHz – 250 MHz[16]
Timebase accuracy	
Phase-locked to onboard clock	±25.0 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy
Duty cycle tolerance	45% to 55%

15. Divide by n decimation from 250 MS/s. For more information about the sample clock and decimation, refer to the ***NI Reconfigurable Oscilloscopes Help*** at ni.com/manuals.
16. Variable external sample clock support was added in NI-SCOPE 18.7.

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard clock (internal VCXO) PXI_Clk10 (backplane connector)
External (10 MHz)	AUX I/O CLK IN (front panel MHDMR connector)
Duty cycle tolerance	45% to 55%

External Sample Clock

Source	AUX I/O CLK IN (front panel MHDMR connector)
Impedance	50 Ω
Coupling	AC
Input voltage range	
As a 250 MHz sine wave	1 dBm through 18 dBm
As a fast slew rate input (square wave, V_{pk-pk})	0.4 V to 5 V
Maximum input overload	
As a 250 MHz sine wave	20 dBm

As a fast slew rate input (square wave, V_{pk-pk})	6 V

External Reference Clock In

Source	AUX I/O CLK IN (front panel MHDMR connector)
Impedance	50 Ω
Coupling	AC
Frequency[17]	10 MHz
Input voltage range	
As a 250 MHz sine wave	1 dBm through 18 dBm
As a fast slew rate input (square wave, V_{pk-pk})	6 V
Duty cycle tolerance	45% to 55%

Reference Clock Out

Source	PXI_Clk10 (backplane connector)
Destination	AUX I/O CLK OUT (front panel MHDMR connector)

17. The PLL reference clock frequency must be accurate to ±25 ppm.

Output impedance	50 Ω
Logic type	3.3 V LVCMOS
Maximum current drive	±8 mA

PXIe_DStarA

Source	System timing slot
Destinations	Onboard clock (internal VCXO) FPGA

PXI_Clk100

Source	PXI backplane
Destination	FPGA

Trigger

Note The following characteristic behaviors are valid when using the device with the NI-SCOPE API. When using instrument design libraries, these characteristics may not be valid.

Supported trigger	Reference (Stop) Trigger

Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 to CH 7 PFI <0..7> PXI_Trig <0..6> Software
Time resolution	
Analog triggers	
With interpolation	Sample Clock period / 1024
Without interpolation	Sample Clock period
Digital triggers	2x Sample Clock period
Approximate trigger delay difference between analog edge trigger and digital trigger source[18]	630 ns, nominal

18. This value is approximate because changes to the digital trigger routing or the analog signal path affect propagation delay. You can compensate for the delay difference by adjusting the NI-SCOPE trigger delay value. Add an additional 80 ns trigger delay when passing a trigger between PXIe-5171 modules. With the same hardware and software configuration, the trigger delay difference is

Minimum dead time	
With interpolation	240 x Sample Clock period
Without interpolation	130 x Sample Clock period

Holdoff	From dead time to [$(2^{64} - 1) \times$ Sample Clock timebase period]
Trigger delay	From 0 to [$(2^{51} - 1) \times$ Sample Clock timebase period]
Analog trigger accuracy with input frequencies less than 90 MHz	0.5% of full scale
Analog trigger jitter with input frequencies less than 90 MHz	15 ps_{rms}
Minimum threshold duration[19]	Sample Clock period

Note Trigger interpolation is used when the Enable TDCNI-SCOPE attribute is set to `TRUE`. Otherwise, trigger interpolation is not used.

For more information about triggers, refer to ***Triggering*** in ***NI-SCOPE***.

consistent within the timing resolution across modules of the same model. For more information about the trigger delay difference, refer to ***Characterizing Setup to Account for Delay on Digital Trigger***.

19. Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

Related information:

- Triggering
- Characterizing Setup to Account for Delay on Digital Trigger

Programmable Function Interface (PFI 0..7, AUX I/O Front Panel Connector)

Connector	AUX I/O
Direction	Bidirectional per channel
Direction control latency	25 ns
As an Input (Trigger)	
Destination	FPGA diagram Start Trigger (Acquisition Arm) Reference (Stop) Trigger Arm Reference Trigger Advance Trigger
Input impedance	10 kΩ
V_{IH}	2 V
V_{IL}	0.8 V

Maximum input overload	0 V to 3.3 V, 5 V tolerant
Minimum pulse width	10 ns
As an Output (Event)	
Sources	FPGA diagram Ready for Start Start Trigger (Acquisition Arm) Ready for Reference Reference (Stop) Trigger End of Record Ready for Advance Advance Trigger Done (End of Acquisition)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Minimum pulse width	10 ns

Power Output (+3.3 V)

Connector	AUX I/O/+3.3 V front panel connector
Voltage output	3.3 V ± 10%
Maximum current drive	200 mA
Output impedance	<1 Ω

Waveform Specifications

Onboard memory size[20]	1.5 GB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (record length - 1)
Number of posttrigger samples	Zero up to record length

Channels	Max Records per Channel	Record Length
1	1	805306192
1	10	80530432
1	1000	805120
1	100,000	7840

20. Onboard memory is shared among all enabled channels.

Channels	Max Records per Channel	Record Length
1	1M	592
2	1	402653096
2	10	40265216
2	1000	402560
2	100,000	3920
2	1M	296
4	1	201326548
4	10	20132608
4	1000	201280
4	100,000	1960
4	1M	148
8	1	100663274
8	10	10066304
8	1000	100640
8	100,000	980
8	1M	74

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at ni.com/manuals.

FPGA

FPGA support	Xilinx Kintex-7 XC7K410T FPGA
Xilinx Kintex-7 XC7K410T FPGA Resources	
Slice registers	508,400

Slice look-up tables (LUT)	254,200
DSPs	1,540
18 Kb block RAMs	1,590

Note Note that some of these resources are consumed by the logic necessary to operate the device and integrate with software, and are thus out of the control of users.

External Calibration

External calibration corrects for gain, offset, and timing errors at all input ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for intermodule synchronization errors.

For information about when to self-calibrate the device, refer to the documentation of your device at ni.com.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[21]	15 minutes

21. Warm-up begins after the chassis is powered, the device is recognized by the host, and the device is configured using the instrument design libraries or NI-SCOPE. Running an included sample project or

Software

Driver Software

This device was first supported in LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes 14.0 and NI-SCOPE 15.1. NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the device. NI-SCOPE provides application programming interfaces for many development environments.

For information about the available software options, refer to the documentation of your device at ni.com.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5171 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5171 was first available via InstrumentStudio in

running self-calibration using NI-MAX will configure the device and start warm-up.

NI-SCOPE18.1 and via the NI-SCOPE SFP in NI-SCOPE15.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5171. MAX is included on the driver media.

Synchronization

Channel-to-channel skew	
Anti-alias filter enabled	<120 ps, nominal[22]
Full bandwidth	<120 ps, nominal

Synchronization with the NI-TClk API

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5171 and NI-SCOPE.
NI-TClk installs with NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PXIe-5171 modules using NI-TClk [23]	
NI-TClk synchronization without manual adjustment [24] [24]	
Skew, Peak-to-Peak [25] [25]	300 ps
NI-TClk synchronization with manual adjustment [24]	
Skew after manual adjustment	≤10 ps

22. For input frequencies less than 75 MHz.

Sample Clock delay/adjustment resolution	3.5 ps

Power

Note Power consumed depends on the FPGA image and driver software used. This specifications represents the maximum power for the NI-SCOPE use case or the typical value when using the Instrument Design Libraries (IDL).

Table 12. PXIe-5171 Power Consumption

	Instrument Design Libraries	NI-SCOPE
+3.3 VDC	6.4 W	6.3 W
+12 VDC	16.2W	17.2W
Total power	22.6 W	23.5 W

Total maximum power allowed	38.25 W

23. Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules. Specifications are valid under the following conditions:

    - All modules installed in the same PXI Express chasses.
    - NI-TClk used to align the sample clocks of each module.
    - All parameters set to identical values for each module.
    - Self-calibration completed.
    - Ambient temperature within ±1 °C of self-calibration.

    For other configurations, including multi-chassis systems, contact NI Technical Support at ***ni.com/support***.
24. Manual adjustment is the process of minimizing synchronization jitter and skew by adjusting Trigger Clock (TClk) signals using the instrument driver.
25. Caused by clock and analog delay differences. Tested with a PXIe-1082 chassis with maximum slot to slot skew of 100 ps. Valid within ±1 °C of self-calibration.

Dimensions and Weight

Dimensions	18.5 cm × 2.0 cm × 13.0 cm (7.3 in. × 0.8 in. × 5.1 in.) 3U, 1 slot, PXI Express Gen 2 x8 Module

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 40 °C
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C
Relative humidity range	5% to 95%, noncondensing

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g RMS
Nonoperating	5 Hz to 500 Hz, 2.4 g RMS

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions

- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the ***Engineering a Healthy Planet*** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region,

visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国RoHS）

- **中国RoHS**— NI符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于NI中国RoHS合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)